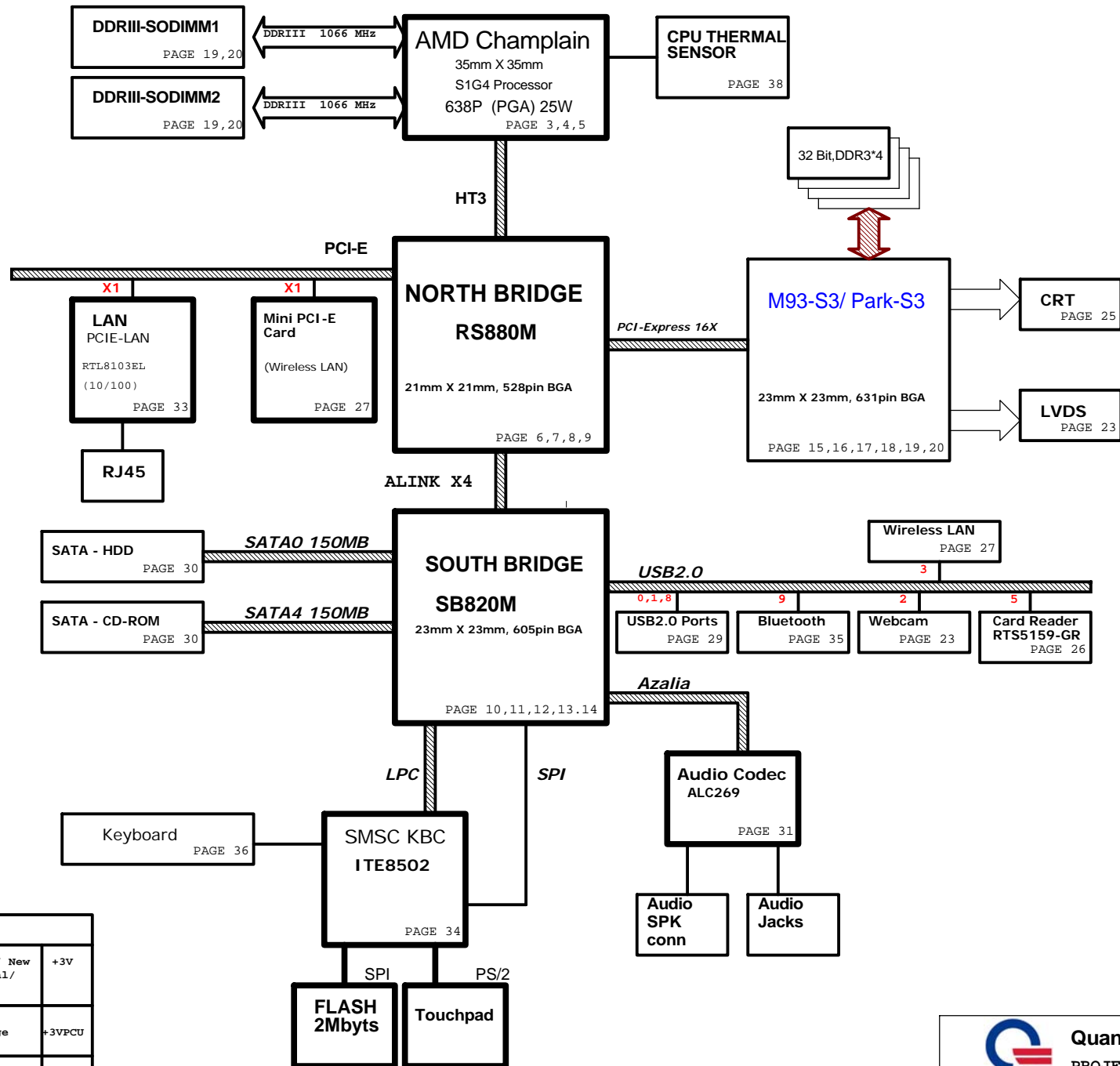
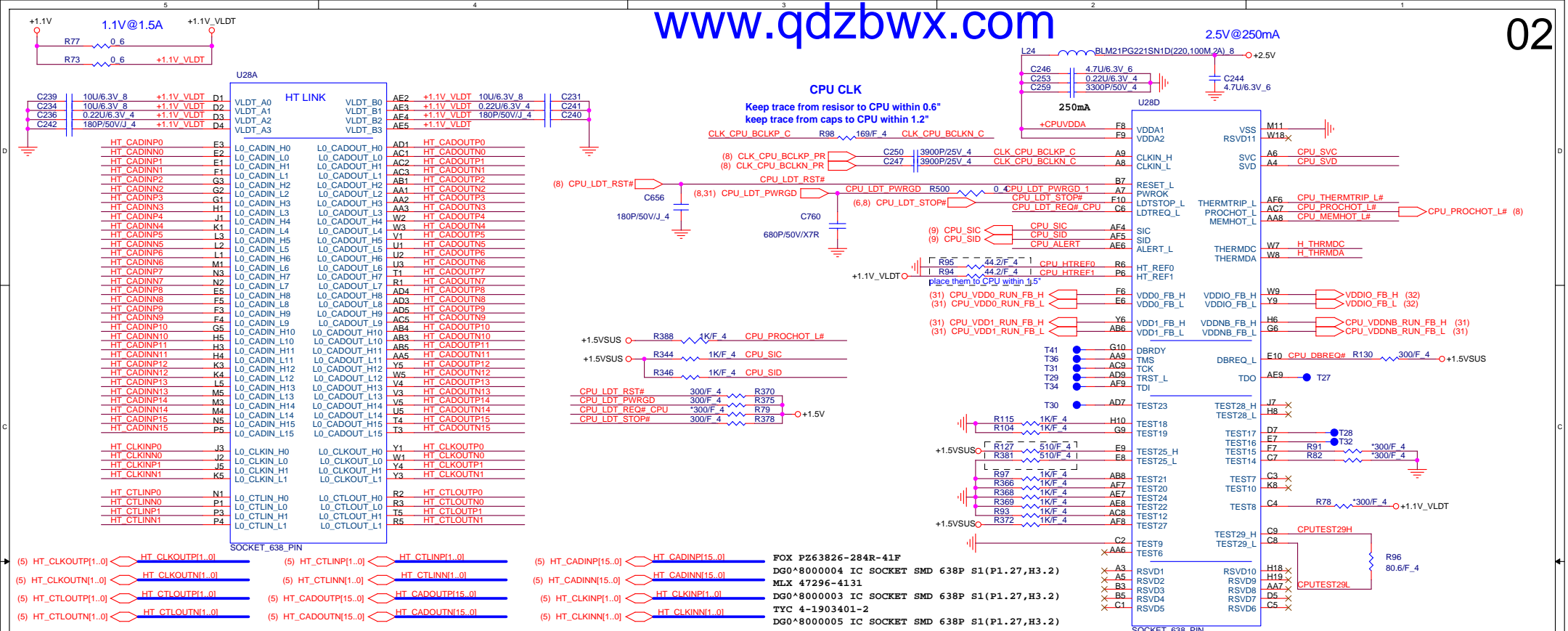


PCB STACK UP

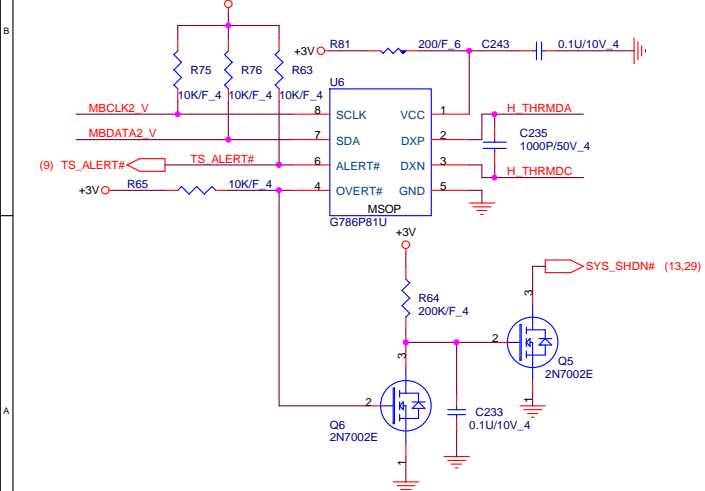
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



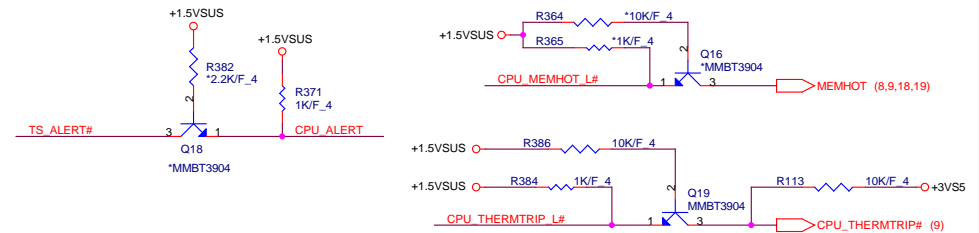
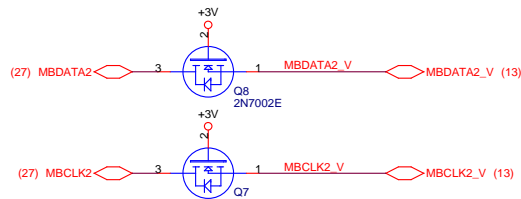
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/ wireless LAN/ New card/ DDR3/ DDR3 thermal/ Accelerometer/system thermal	+3V
EC -- AB1A	Battery charge/discharge	+3VPCU
EC -- AB2A	VGA thermal	+3V



+3V CPU Thermal Sensor

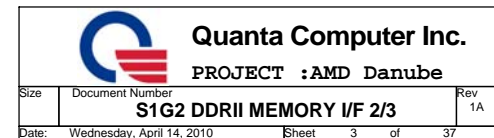


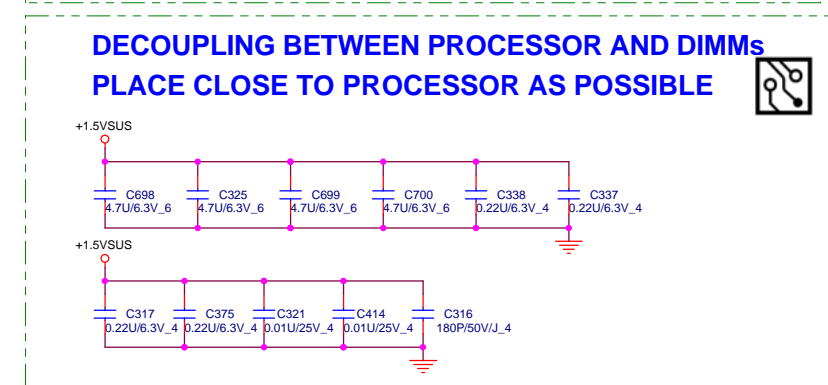
MBCLK2/MBDATA2	
G786P81U	1001 100X
G781-1P8	1001 101X



Serial VID

VFIX MODE		VID Override Circuit
SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V





This block is for UMA only , Discrete can remove all component

PART 1 OF 6

HYPER TRANSPORT CPU
I/F

U27A

HT_CADOUTP0	Y26	HT_RXCAD0P	D24	HT_CADINP0
HT_CADOUTN0	Y24	HT_RXCAD0N	D25	HT_CADINN0
HT_CADOUTP1	V22	HT_RXCAD1P	E24	HT_CADINP1
HT_CADOUTN1	V23	HT_RXCAD1N	E25	HT_CADINN1
HT_CADOUTP2	V25	HT_RXCAD2P	D24	HT_CADINP2
HT_CADOUTN2	V24	HT_RXCAD2N	E25	HT_CADINN2
HT_CADOUTP3	U24	HT_RXCAD3P	E25	HT_CADINP3
HT_CADOUTN3	U25	HT_RXCAD3N	E22	HT_CADINN3
HT_CADOUTP4	T25	HT_RXCAD3P	H23	HT_CADINP4
HT_CADOUTN4	T24	HT_RXCAD4P	H22	HT_CADINN4
HT_CADOUTP5	P22	HT_RXCAD4P	J25	HT_CADINP5
HT_CADOUTN5	P23	HT_RXCAD4N	J25	HT_CADINN5
HT_CADOUTP6	P24	HT_RXCAD5P	J24	HT_CADINP6
HT_CADOUTN6	P24	HT_RXCAD5N	K24	HT_CADINP7
HT_CADOUTP7	N24	HT_RXCAD6P	K25	HT_CADINN6
HT_CADOUTN7	N25	HT_RXCAD6N	K23	HT_CADINP7
		HT_RXCAD7P	K22	HT_CADINN7
		HT_RXCAD7N		

HT_CADOUTP8	AC24	HT_RXCAD8P	E21	HT_CADINP8
HT_CADOUTN8	AB25	HT_RXCAD8N	G21	HT_CADINN8
HT_CADOUTP9	AB24	HT_RXCAD9P	G20	HT_CADINP9
HT_CADOUTN9	AB24	HT_RXCAD9N	H21	HT_CADINP9
HT_CADOUTP10	AA24	HT_RXCAD9N	J20	HT_CADINP10
HT_CADOUTN10	AA25	HT_RXCAD10P	J21	HT_CADINN10
HT_CADOUTP11	Y22	HT_RXCAD10N	J18	HT_CADINP11
HT_CADOUTN11	Y23	HT_RXCAD11P	K17	HT_CADINN11
HT_CADOUTP12	V21	HT_RXCAD11N	L19	HT_CADINP12
HT_CADOUTN12	V20	HT_RXCAD12P	J19	HT_CADINN12
HT_CADOUTP13	V21	HT_RXCAD12N	M19	HT_CADINP13
HT_CADOUTN13	V20	HT_RXCAD13P	L18	HT_CADINN13
HT_CADOUTP14	U20	HT_RXCAD14P	M21	HT_CADINP14
HT_CADOUTN14	U21	HT_RXCAD14N	P21	HT_CADINN14
HT_CADOUTP15	U19	HT_RXCAD15P	P18	HT_CADINP15
HT_CADOUTN15	U18	HT_RXCAD15N	M18	HT_CADINN15

HT_CLKOUTP0	T22	HT_RXCLK0P	H24	HT_CLKINP0
HT_CLKOUTN0	T23	HT_RXCLK0N	H25	HT_CLKINN0
HT_CLKOUTP1	AB23	HT_RXCLK1P	L21	HT_CLKINP1
HT_CLKOUTN1	AB22	HT_RXCLK1N	L20	HT_CLKINN1

HT_CTLOUTP0	M22	HT_RXCTL0P	M24	HT_CTLINP0
HT_CTLOUTN0	M23	HT_RXCTL0N	M25	HT_CTLINN0
HT_CTLOUTP1	R21	HT_RXCTL1P	P19	HT_CTLINP1
HT_CTLOUTN1	R20	HT_RXCTL1N	P18	HT_CTLINN1

HT_RXCALP	C23	HT_TXCALP	B24	HT_TXCALP
HT_RXCALN	A24	HT_TXCALN	B25	HT_TXCALN

RS880M

PART 2 OF 6

PCIe I/F
GFX

U27B

(12) PEG_RXP15	D4	GFX_RX0P	A5	PEG_TXP15_C	C606	0.1U/10V_4	PEG_TXP15 (12)
(12) PEG_RXN15	C4	GFX_RX0N	B5	PEG_TXN15_C	C607	0.1U/10V_4	PEG_TXN15 (12)
(12) PEG_RXP14	A3	GFX_RX1P	A4	PEG_TXP14_C	C604	0.1U/10V_4	PEG_TXP14 (12)
(12) PEG_RXN14	B3	GFX_RX1N	B4	PEG_TXN14_C	C605	0.1U/10V_4	PEG_TXN14 (12)
(12) PEG_RXP13	C2	GFX_RX2P	C3	PEG_TXP13_C	C603	0.1U/10V_4	PEG_TXP13 (12)
(12) PEG_RXN13	C1	GFX_RX2N	B2	PEG_TXN13_C	C602	0.1U/10V_4	PEG_TXN13 (12)
(12) PEG_RXP12	E5	GFX_RX3P	D1	PEG_TXP12_C	C600	0.1U/10V_4	PEG_TXP12 (12)
(12) PEG_RXN12	E5	GFX_RX3N	D2	PEG_TXN12_C	C601	0.1U/10V_4	PEG_TXN12 (12)
(12) PEG_RXP11	G5	GFX_RX4P	E2	PEG_TXP11_C	C599	0.1U/10V_4	PEG_TXP11 (12)
(12) PEG_RXN11	G6	GFX_RX4N	E1	PEG_TXN11_C	C598	0.1U/10V_4	PEG_TXN11 (12)
(12) PEG_RXP10	H5	GFX_RX5P	F4	PEG_TXP10_C	C597	0.1U/10V_4	PEG_TXP10 (12)
(12) PEG_RXN10	H6	GFX_RX5N	F3	PEG_TXN10_C	C596	0.1U/10V_4	PEG_TXN10 (12)
(12) PEG_RXP9	J5	GFX_RX6P	F1	PEG_TXP9_C	C616	0.1U/10V_4	PEG_TXP9 (12)
(12) PEG_RXN9	J6	GFX_RX6N	F2	PEG_TXN9_C	C619	0.1U/10V_4	PEG_TXN9 (12)
(12) PEG_RXP8	J7	GFX_RX7P	H4	PEG_TXP8_C	C622	0.1U/10V_4	PEG_TXP8 (12)
(12) PEG_RXN8	J8	GFX_RX7N	H3	PEG_TXN8_C	C625	0.1U/10V_4	PEG_TXN8 (12)
(12) PEG_RXP7	L5	GFX_RX8P	H1	PEG_TXP7_C	C626	0.1U/10V_4	PEG_TXP7 (12)
(12) PEG_RXN7	L6	GFX_RX8N	H2	PEG_TXN7_C	C629	0.1U/10V_4	PEG_TXN7 (12)
(12) PEG_RXP6	M8	GFX_RX9P	J2	PEG_TXP6_C	C630	0.1U/10V_4	PEG_TXP6 (12)
(12) PEG_RXN6	L8	GFX_RX9N	J1	PEG_TXN6_C	C633	0.1U/10V_4	PEG_TXN6 (12)
(12) PEG_RXP5	P7	GFX_RX10P	K4	PEG_TXP5_C	C634	0.1U/10V_4	PEG_TXP5 (12)
(12) PEG_RXN5	M7	GFX_RX10N	K3	PEG_TXN5_C	C636	0.1U/10V_4	PEG_TXN5 (12)
(12) PEG_RXP4	P5	GFX_RX11P	K1	PEG_TXP4_C	C637	0.1U/10V_4	PEG_TXP4 (12)
(12) PEG_RXN4	M5	GFX_RX11N	K2	PEG_TXN4_C	C638	0.1U/10V_4	PEG_TXN4 (12)
(12) PEG_RXP3	R8	GFX_RX12P	M4	PEG_TXP3_C	C639	0.1U/10V_4	PEG_TXP3 (12)
(12) PEG_RXN3	R6	GFX_RX12N	M3	PEG_TXN3_C	C640	0.1U/10V_4	PEG_TXN3 (12)
(12) PEG_RXP2	R5	GFX_RX13P	M1	PEG_TXP2_C	C641	0.1U/10V_4	PEG_TXP2 (12)
(12) PEG_RXN2	P4	GFX_RX13N	N2	PEG_TXN2_C	C642	0.1U/10V_4	PEG_TXN2 (12)
(12) PEG_RXP1	P3	GFX_RX14P	N1	PEG_TXN1_C	C644	0.1U/10V_4	PEG_TXN1 (12)
(12) PEG_RXN1	T4	GFX_RX14N	P1	PEG_TXP0_C	C654	0.1U/10V_4	PEG_TXP0 (12)
(12) PEG_RXP0	T3	GFX_RX15P	P2	PEG_TXN0_C	C655	0.1U/10V_4	PEG_TXN0 (12)
(12) PEG_RXN0	T3	GFX_RX15N					

(26) PCIe_RXP0_LAN	AE3	GPP_RX0P	AC1	PCIe_TXP0_LAN_C	C660	0.1U/10V_4	PCIe_TXP0_LAN (26)
(26) PCIe_RXN0_LAN	AD4	GPP_RX0N	AC2	PCIe_TXN0_LAN_C	C662	0.1U/10V_4	PCIe_TXN0_LAN (26)
(23) PCIe_RXP1	AE2	GPP_RX1P	AB4	PCIe_TXP1_C	C658	0.1U/10V_4	PCIe_TXP1 (23)
(23) PCIe_RXN1	AD3	GPP_RX1N	AB3	PCIe_TXN1_C	C659	0.1U/10V_4	PCIe_TXN1 (23)

PCIe I/F GPP

(8) A_RXP0	AA8	SB_RX0P	AD7	A_TXP0_C	C669	0.1U/10V_4	A_TXP0 (8)
(8) A_RXN0	Y8	SB_RX0N	AE7	A_TXN0_C	C670	0.1U/10V_4	A_TXN0 (8)
(8) A_RXP1	AA7	SB_RX1P	AE6	A_TXP1_C	C667	0.1U/10V_4	A_TXP1 (8)
(8) A_RXN1	Y7	SB_RX1N	AD6	A_TXN1_C	C668	0.1U/10V_4	A_TXN1 (8)
(8) A_RXP2	AA5	SB_RX2P	AB6	A_TXN2_C	C671	0.1U/10V_4	A_TXN2 (8)
(8) A_RXN2	AA6	SB_RX2N	AD5	A_TXP3_C	C672	0.1U/10V_4	A_TXP3 (8)
(8) A_RXP3	Y6	SB_RX3P	AE5	A_TXN3_C	C674	0.1U/10V_4	A_TXN3 (8)
(8) A_RXN3	Y5	SB_RX3N					

PCIe I/F SB

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

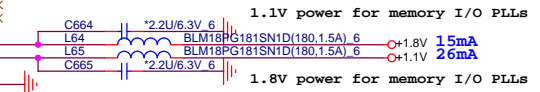
RS880M

AC8	NB_PCIECALRP	R71	1.27K Ω 4	+1.1V
AB8	NB_PCIECALRN	R72	2K Ω 4	

PAR 4 OF 6

AB12	MEM_A0(NC)	MEM_DQ0/DV0_VSYNC(NC)	AA18	
AE16	MEM_A1(NC)	MEM_DQ1/DV0_HSYNC(NC)	AA20	
V11	MEM_A2(NC)	MEM_DQ2/DV0_DE(NC)	AA19	
AA15	MEM_A3(NC)	MEM_DQ3/DV0_DO(NC)	V17	
AB16	MEM_A4(NC)	MEM_DQ4(NC)	AA17	
AB14	MEM_A5(NC)	MEM_DQ5/DV0_D1(NC)	AA15	
AD14	MEM_A7(NC)	MEM_DQ7/DV0_D4(NC)	V15	
AD13	MEM_A8(NC)	MEM_DQ8/DV0_D3(NC)	AC20	
AD15	MEM_A9(NC)	MEM_DQ9/DV0_D5(NC)	AD19	
AE13	MEM_A10(NC)	MEM_DQ10/DV0_D6(NC)	AC18	
AC14	MEM_A11(NC)	MEM_DQ11/DV0_D7(NC)	AB20	
Y14	MEM_A12(NC)	MEM_DQ12(NC)	AE22	
AD16	MEM_A13(NC)	MEM_DQ13/DV0_D9(NC)	AC22	
AE17	MEM_BA0(NC)	MEM_DQ14/DV0_D10(NC)	AC22	
AD17	MEM_BA1(NC)	MEM_DQ15/DV0_D11(NC)	AD21	
	MEM_BA2(NC)			
W12	MEM_RASB(NC)	MEM_DQS0P/DV0_IDCKP(NC)	Y17	
Y12	MEM_CASB(NC)	MEM_DQS0N/DV0_IDCKN(NC)	W18	
AB18	MEM_WEB(NC)	MEM_DQS1P(NC)	AD20	
AB13	MEM_CSB(NC)	MEM_DQS1N(NC)	AE21	
W14	MEM_CKE(NC)	MEM_DM0(NC)	W17	
V14	MEM_ODT(NC)	MEM_DM1/DV0_D8(NC)	AE19	
V15	MEM_CKP(NC)	IOPLLVD18(NC)	AE23	
W14	MEM_CKN(NC)	IOPLLVD(NC)	AE24	
AE12	MEM_COMPP(NC)	IOPLLVS(NC)	AD23	
AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18	

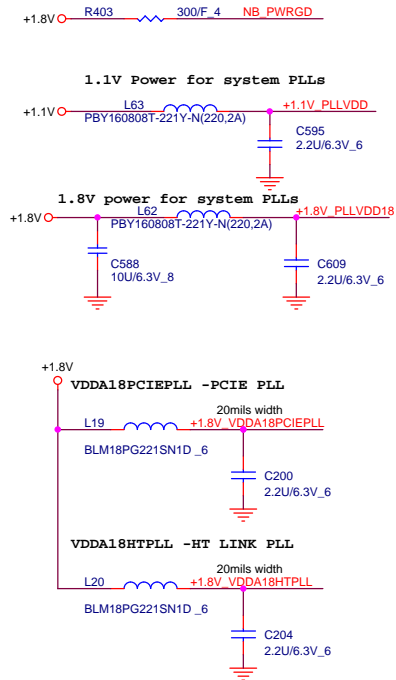
RS880M



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PROJECT :AMD Danube

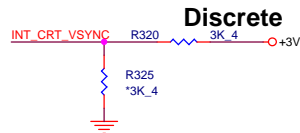
Size	Document Number	Rev
	RS880M LINK I/F 1/3	1A
Date	Wednesday, April 14, 2010	Sheet 5 of 37



Enables Debug Bus access through memory I/O pads and GPIO.

0 : Enable RS880M, Default

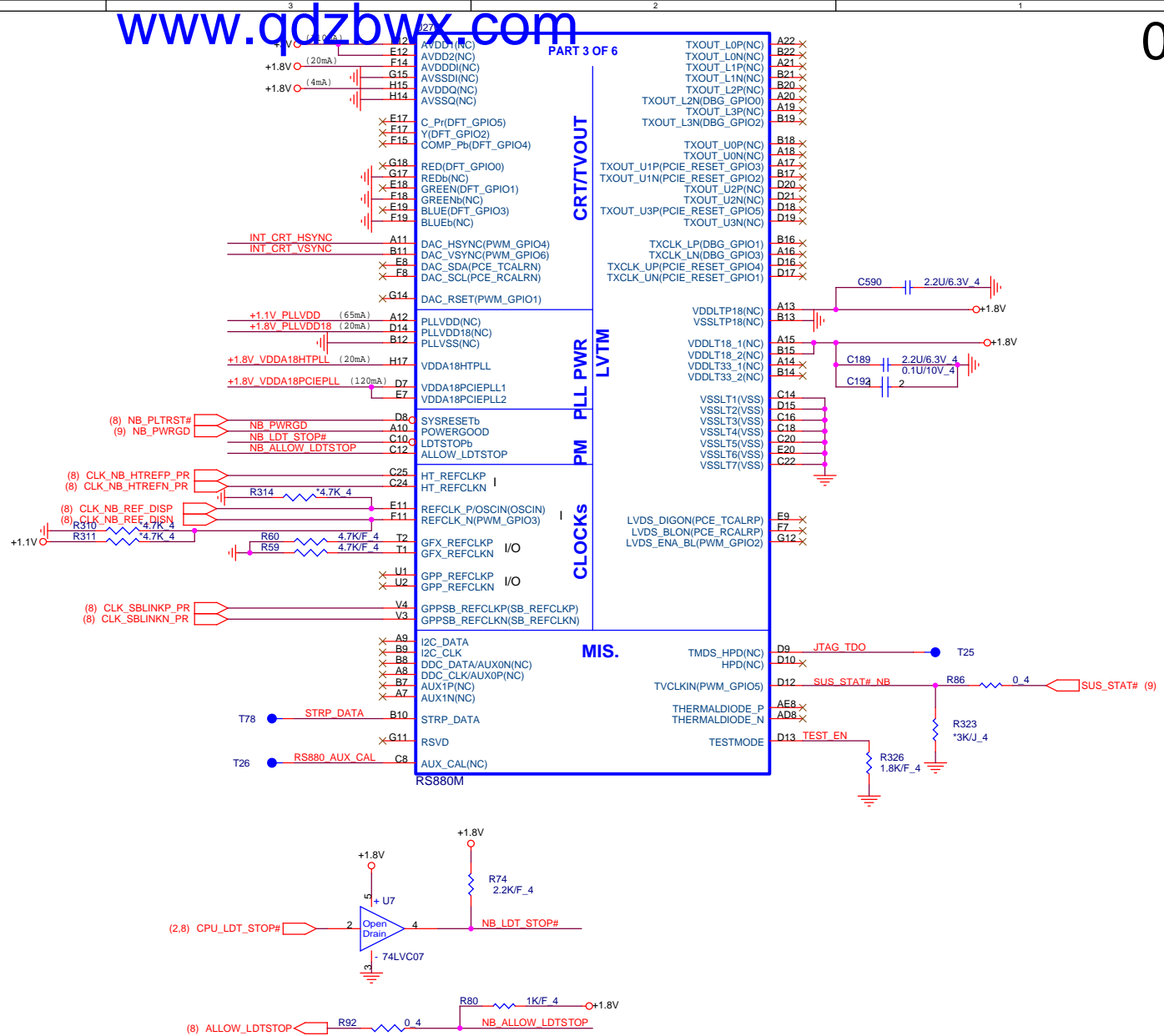
1 : Disable RS880M (RX881 use DAC_VSYN)



Indicates if memory is available or not

0: Available

1: Not available

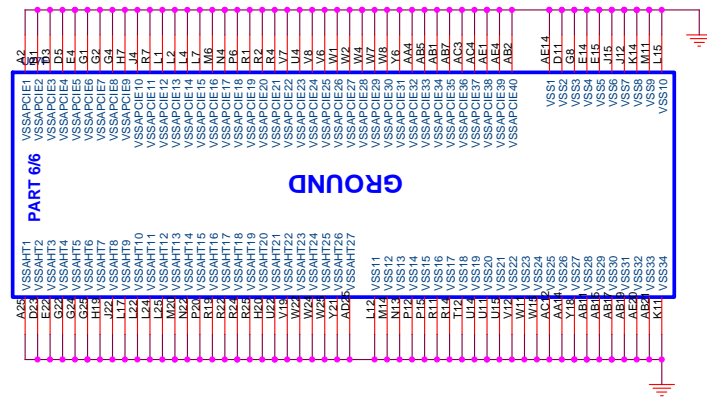


Quanta Computer Inc.

PROJECT :AMD Danube

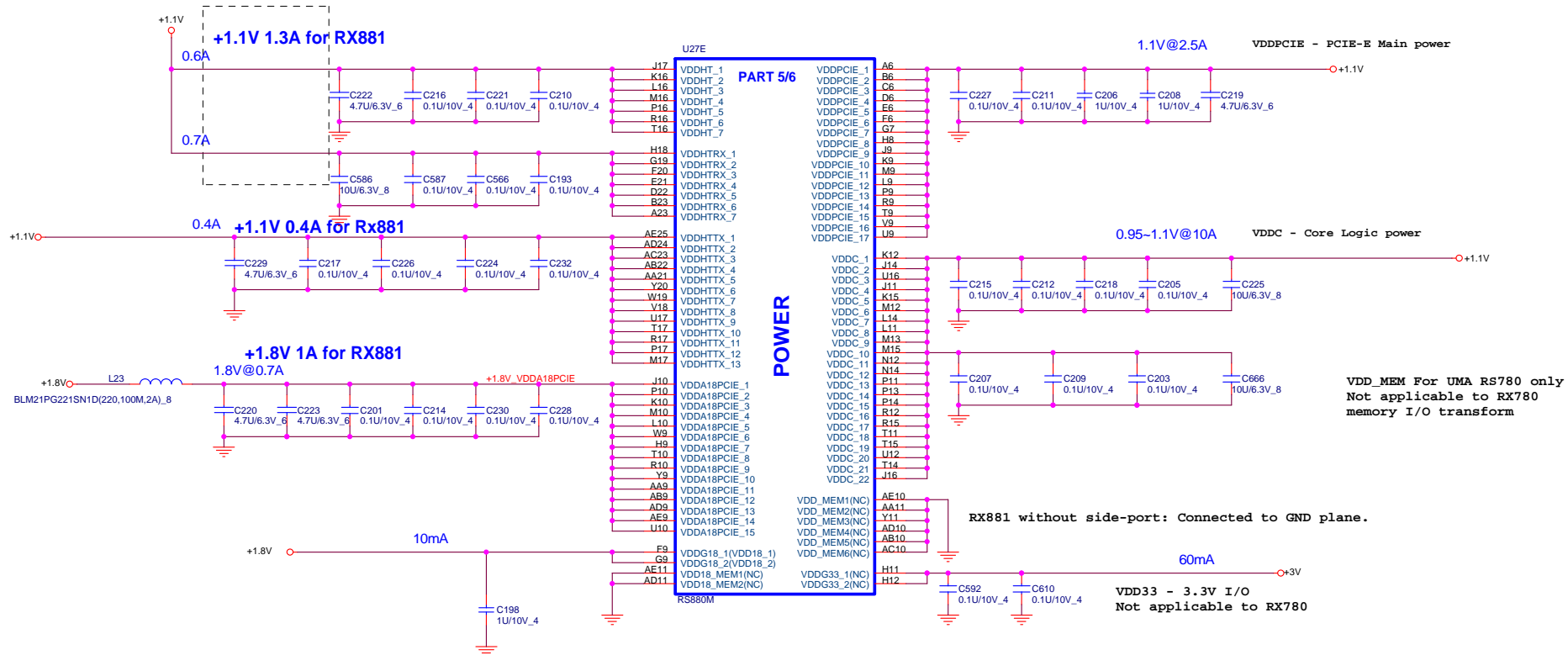
Size Document Number **RS880M-SYSTEM I/F 2/3** Rev 1A

Date: Wednesday, April 14, 2010 Sheet 6 of 37



RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDL18	GND	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDL33	NC	NC

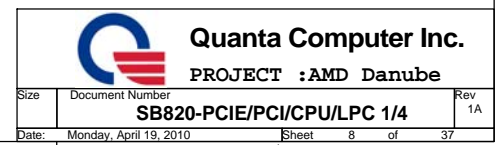


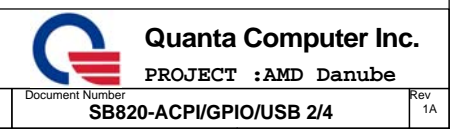
Quanta Computer Inc.

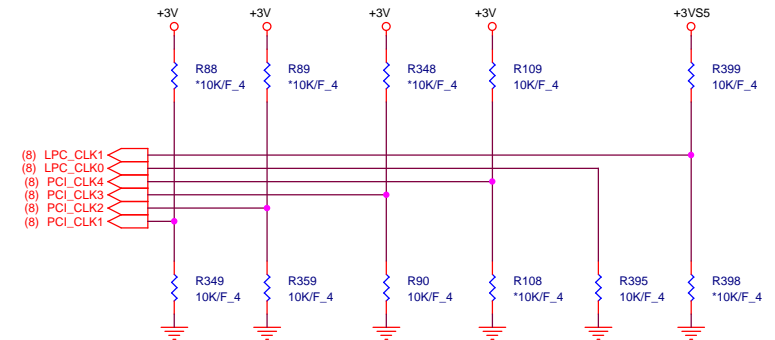
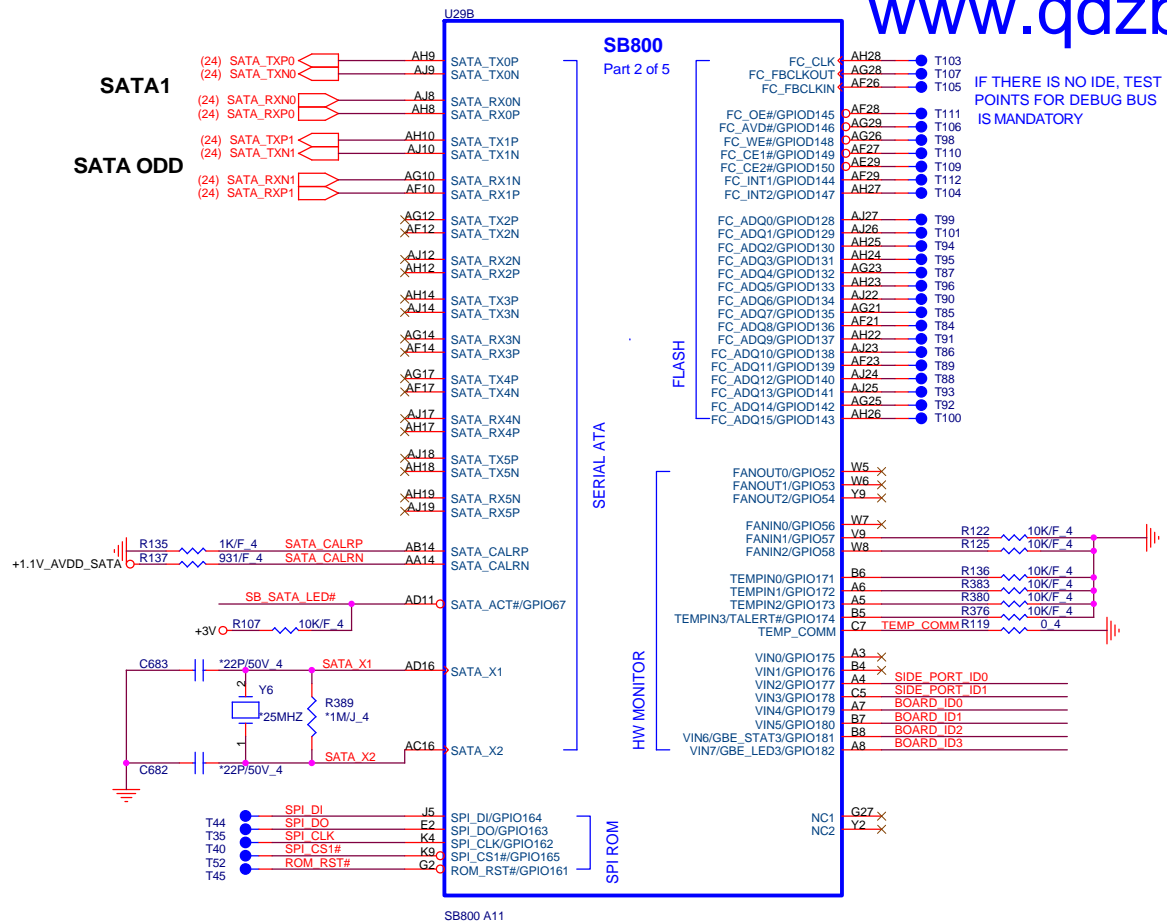
PROJECT :AMD Danube

Size	Document Number	Rev
	RS880M-POWER5 3/3	1A
Date:	Wednesday, March 24, 2010	Sheet 7 of 37

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]







	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT
PULL LOW	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED



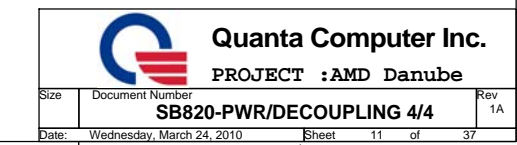
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PROJECT :AMD Danube

Size Document Number
SB820-SATA/IDE/HWM/SPI 3/4 Rev 1A

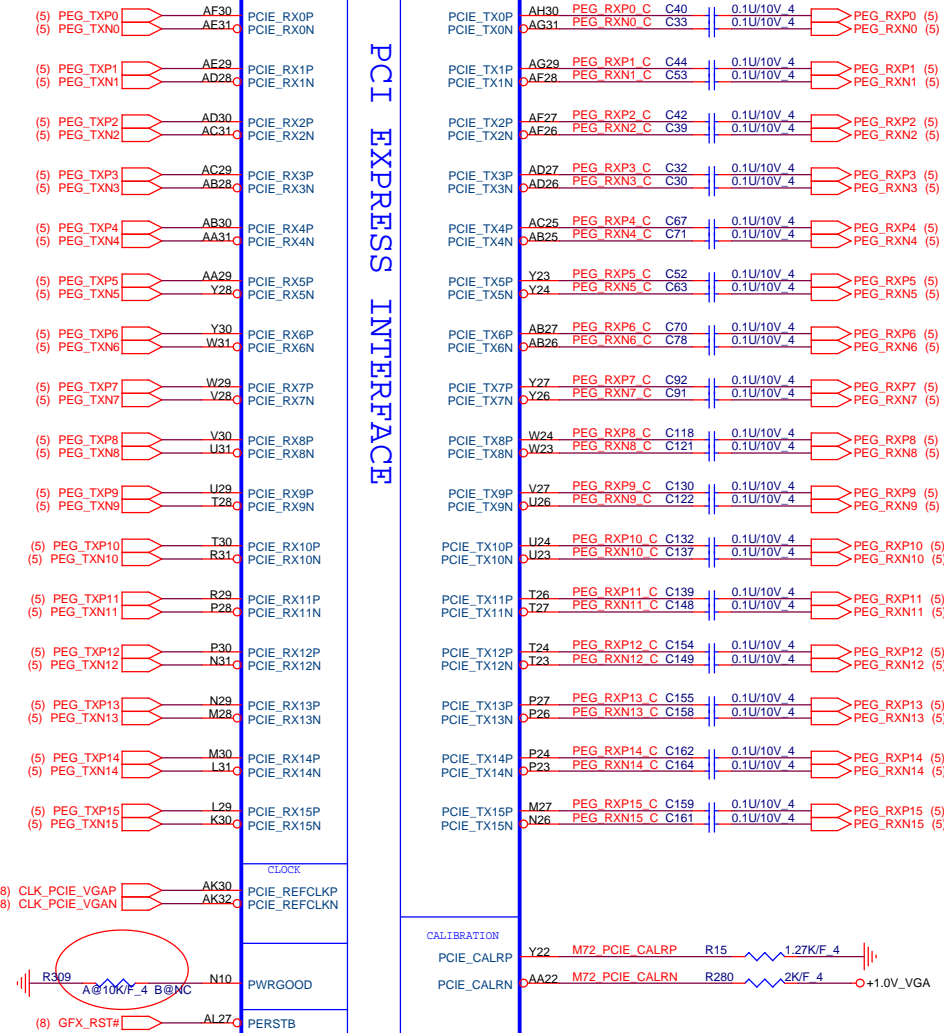
Date: Tuesday, March 23, 2010 Sheet 10 of 37

ID3	ID2	ID1	ID0	
0	0	0	0	FK1 Dis

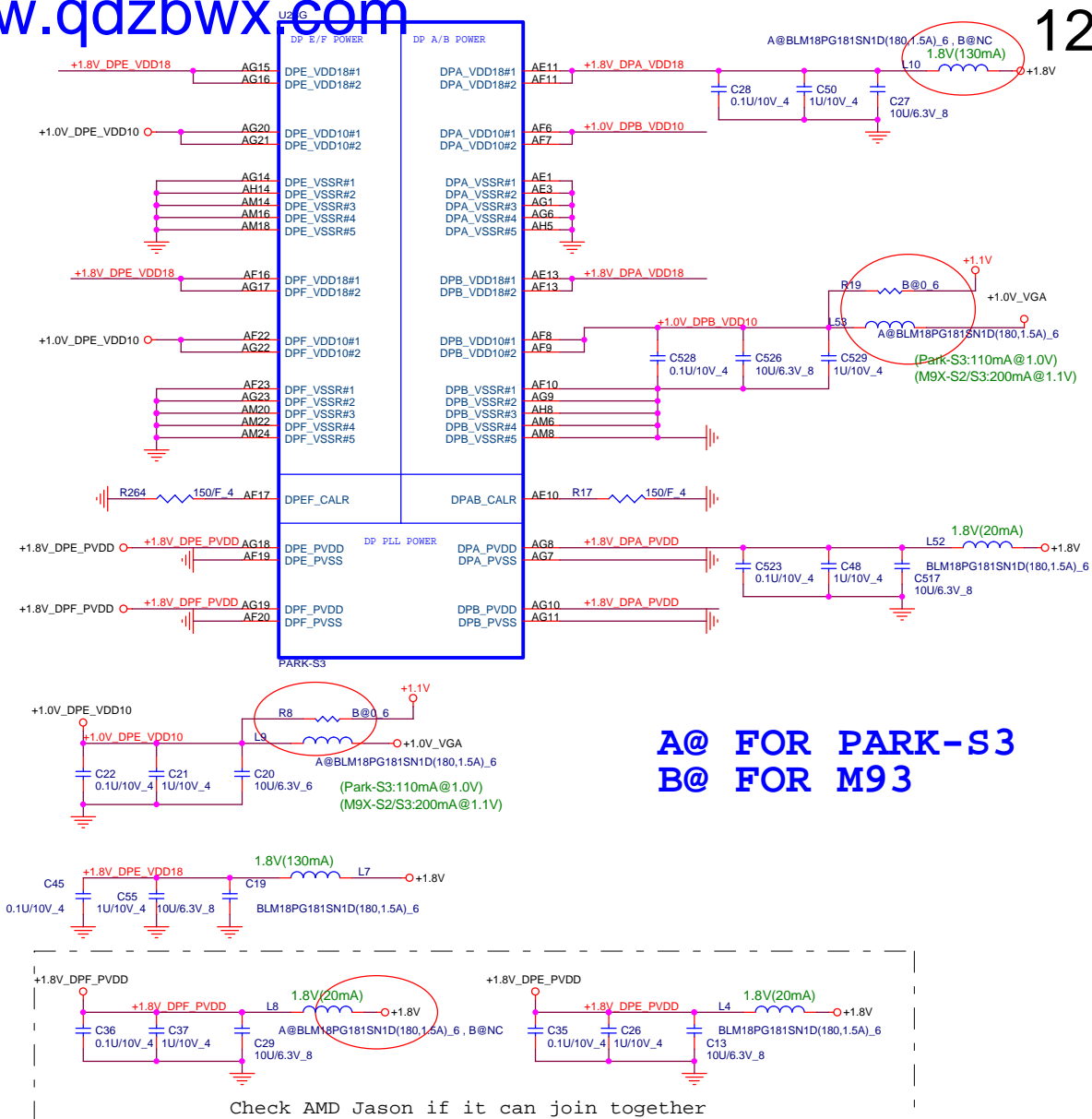


2.5GT/s bit rate

PCI EXPRESS INTERFACE



100MHz (+/-300ppm) input frequency
0-0.7V single-ended swing



PROJECT : AX2/7
Quanta Computer Inc.

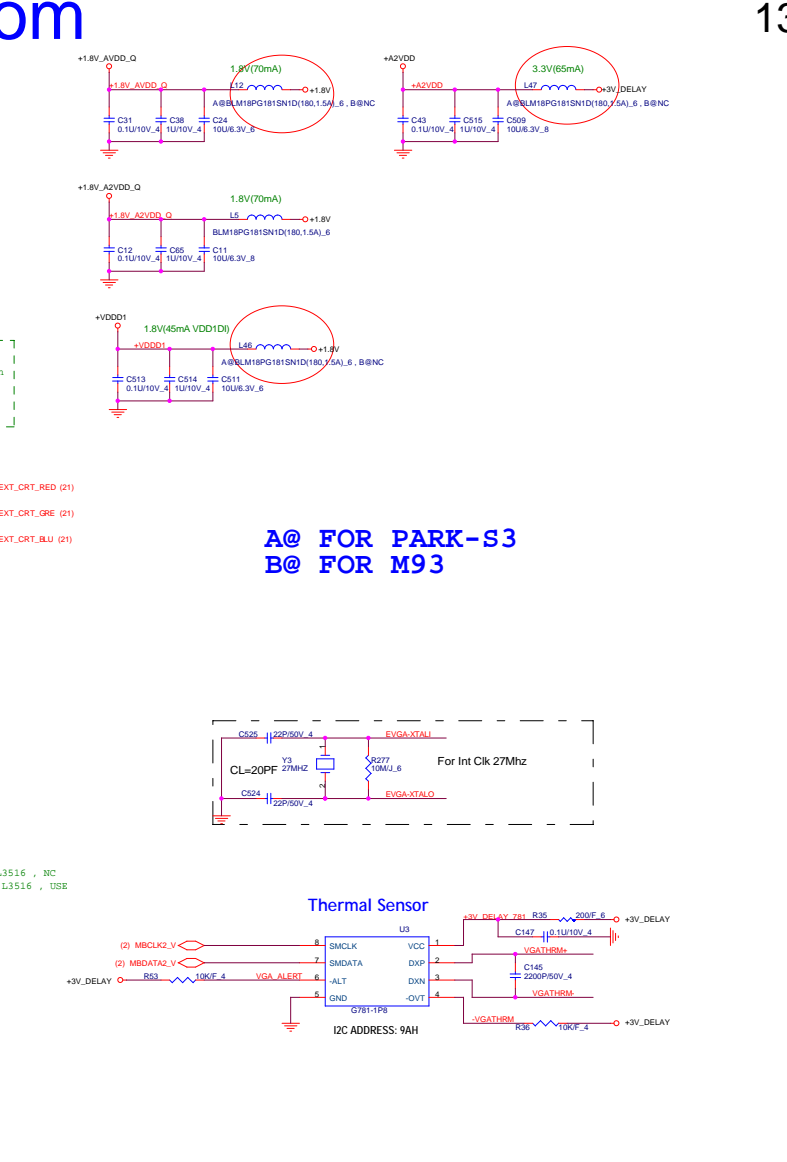
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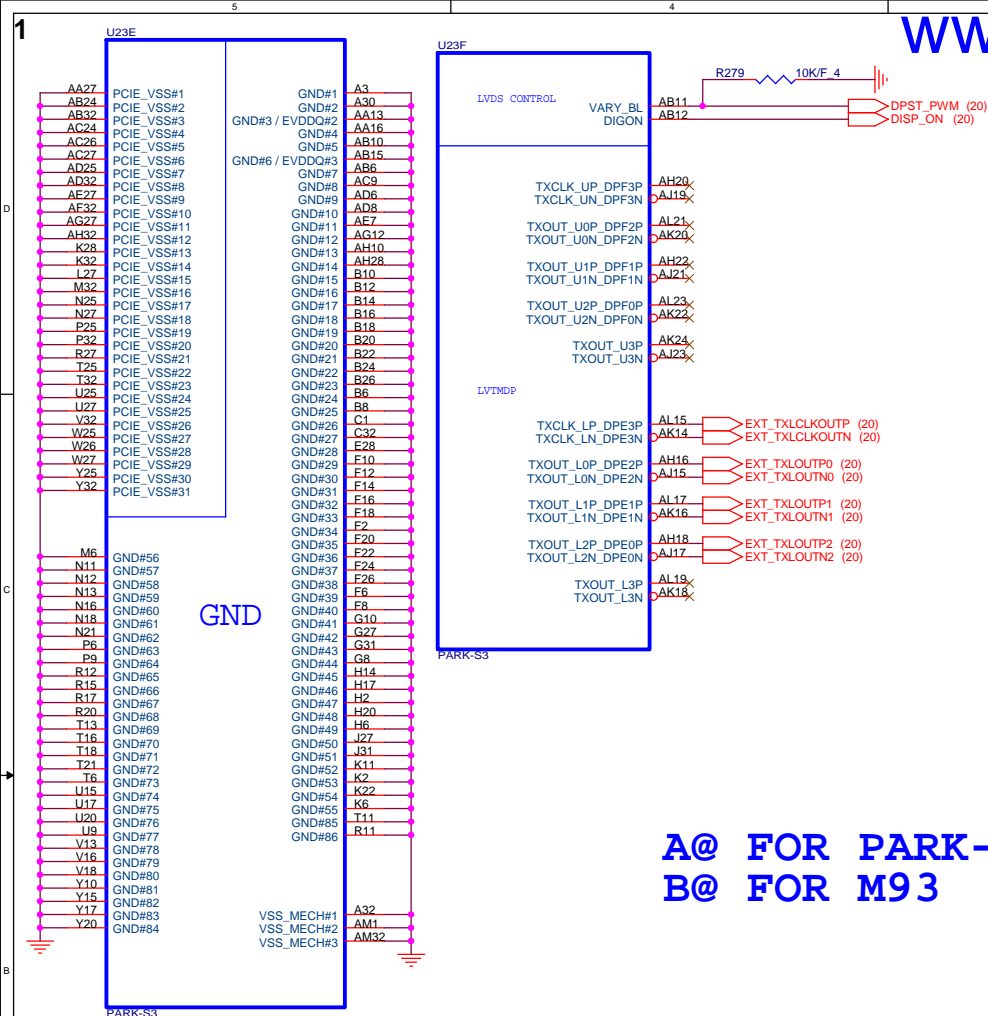
Document Number
PARK_PCIE_Interface

Rev
1A

Date: Tuesday, March 02, 2010 Sheet 12 of 37

PWRCNTL1	V-CORE
1	0.9V
0	0.95V





A@ FOR PARK-S3
B@ FOR M93

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

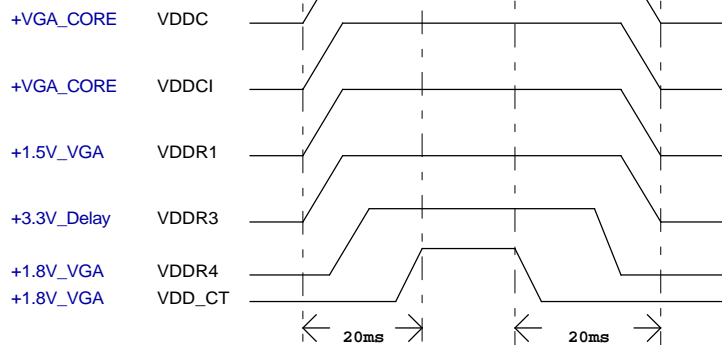
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

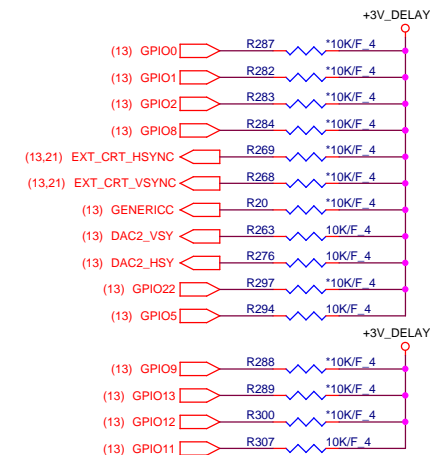
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	512M	0	0	1

Memory Aperture Size 512MB and 256MB GPIO setting is the same
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT : AX2/7
Quanta Computer Inc.

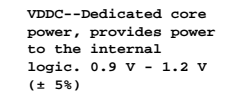
Size
Custom

Document Number
PARK_GND / LVDS/ Straps

Date: Tuesday, April 20, 2010

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Rev
1A



PCIE_VDDC--PCI-E
Digital Power
Supply (Either 1.0
V or 1.1 V) 1.0 V
-5% to 1.1 V +5%

A@ FOR PARK-S3
B@ FOR M93

(17) VMA_WDQS[7..0] <=> VMA_WDQS[7..0]
 (17) VMA_RDQS[7..0] <=> VMA_RDQS[7..0]
 (17) VMA_DM[7..0] <=> VMA_DM[7..0]
 (17) VMA_DQ[63..0] <=> VMA_DQ[63..0]
 (17) VMA_MA[13..0] <=> VMA_MA[13..0]

U23C

VMA_DQ0 K27 DOA_0
 VMA_DQ1 J29 DOA_1
 VMA_DQ2 H30 DOA_2
 VMA_DQ3 H32 DOA_3
 VMA_DQ4 G29 DOA_4
 VMA_DQ5 F28 DOA_5
 VMA_DQ6 F32 DOA_6
 VMA_DQ7 F30 DOA_7
 VMA_DQ8 C30 DOA_8
 VMA_DQ9 F27 DOA_9
 VMA_DQ10 A28 DOA_10
 VMA_DQ11 C28 DOA_11
 VMA_DQ12 E27 DOA_12
 VMA_DQ13 G26 DOA_13
 VMA_DQ14 D26 DOA_14
 VMA_DQ15 F25 DOA_15
 VMA_DQ16 A25 DOA_16
 VMA_DQ17 C25 DOA_17
 VMA_DQ18 E25 DOA_18
 VMA_DQ19 D24 DOA_19
 VMA_DQ20 E23 DOA_20
 VMA_DQ21 F23 DOA_21
 VMA_DQ22 D22 DOA_22
 VMA_DQ23 F21 DOA_23
 VMA_DQ24 E21 DOA_24
 VMA_DQ25 D20 DOA_25
 VMA_DQ26 F19 DOA_26
 VMA_DQ27 A19 DOA_27
 VMA_DQ28 D18 DOA_28
 VMA_DQ29 F17 DOA_29
 VMA_DQ30 A17 DOA_30
 VMA_DQ31 C17 DOA_31
 VMA_DQ32 E17 DOA_32
 VMA_DQ33 D16 DOA_33
 VMA_DQ34 F15 DOA_34
 VMA_DQ35 A15 DOA_35
 VMA_DQ36 D14 DOA_36
 VMA_DQ37 F13 DOA_37
 VMA_DQ38 A13 DOA_38
 VMA_DQ39 C13 DOA_39
 VMA_DQ40 E11 DOA_40
 VMA_DQ41 A11 DOA_41
 VMA_DQ42 C11 DOA_42
 VMA_DQ43 F11 DOA_43
 VMA_DQ44 A9 DOA_44
 VMA_DQ45 C8 DOA_45
 VMA_DQ46 F9 DOA_46
 VMA_DQ47 D8 DOA_47
 VMA_DQ48 E7 DOA_48
 VMA_DQ49 A7 DOA_49
 VMA_DQ50 G7 DOA_50
 VMA_DQ51 F7 DOA_51
 VMA_DQ52 A5 DOA_52
 VMA_DQ53 E5 DOA_53
 VMA_DQ54 C3 DOA_54
 VMA_DQ55 F1 DOA_55
 VMA_DQ56 G7 DOA_56
 VMA_DQ57 G6 DOA_57
 VMA_DQ58 G1 DOA_58
 VMA_DQ59 G3 DOA_59
 VMA_DQ60 J6 DOA_60
 VMA_DQ61 J1 DOA_61
 VMA_DQ62 J3 DOA_62
 VMA_DQ63 J5 DOA_63

MEMORY INTERFACE

MAA_0 K17 VMA_MA0
 MAA_1 J20 VMA_MA1
 MAA_2 H23 VMA_MA2
 MAA_3 G23 VMA_MA3
 MAA_4 G24 VMA_MA4
 MAA_5 H24 VMA_MA5
 MAA_6 J19 VMA_MA6
 MAA_7 K19 VMA_MA7
 MAA_8 J14 VMA_MA8
 MAA_9 K14 VMA_MA9
 MAA_10 J11 VMA_MA10
 MAA_11 J13 VMA_MA11
 MAA_12 H11 VMA_MA12
 G11 VMA_BA2
 J16 VMA_BA0
 MAA_13/BA2 VMA_BA2 (17)
 MAA_14/BA0 VMA_BA0 (17)
 L15 VMA_BA1
 MAA_15/BA1 VMA_BA1 (17)

support 1Gbit VRAM (64M X 16)

DQMA_0 E32 VMA_DM0
 DQMA_1 E30 VMA_DM1
 DQMA_2 A21 VMA_DM2
 DQMA_3 C21 VMA_DM3
 DQMA_4 E13 VMA_DM4
 DQMA_5 D12 VMA_DM5
 DQMA_6 E3 VMA_DM6
 DQMA_7 F4 VMA_DM7

RDQSA_0 H28 VMA_RDQS0
 RDQSA_1 C27 VMA_RDQS1
 RDQSA_2 A23 VMA_RDQS2
 RDQSA_3 E19 VMA_RDQS3
 RDQSA_4 E15 VMA_RDQS4
 RDQSA_5 D10 VMA_RDQS5
 RDQSA_6 D6 VMA_RDQS6
 RDQSA_7 G5 VMA_RDQS7

WDQSA_0 H27 VMA_WDQS0
 WDQSA_1 A27 VMA_WDQS1
 WDQSA_2 C23 VMA_WDQS2
 WDQSA_3 C19 VMA_WDQS3
 WDQSA_4 C15 VMA_WDQS4
 WDQSA_5 E9 VMA_WDQS5
 WDQSA_6 C5 VMA_WDQS6
 WDQSA_7 H4 VMA_WDQS7

ODTA0 L18 VMA_ODT0
 ODTA1 K16 VMA_ODT1

CLKA0 H26 VMA_CLKP0
 CLKA0B H25 VMA_CLKN0
 CLKA1 G9 VMA_CLKP1
 CLKA1B H9 VMA_CLKN1

RASA0B G22 VMA_RAS0#
 RASA1B G17 VMA_RAS1#

CASA0B G19 VMA_CAS0#
 CASA1B G16 VMA_CAS1#

CSA0B_0 H22 VMA_CS0#
 CSA0B_1 J22 VMA_CS1#

CSA1B_0 G13 VMA_CS1#
 CSA1B_1 K13 VMA_CS1#

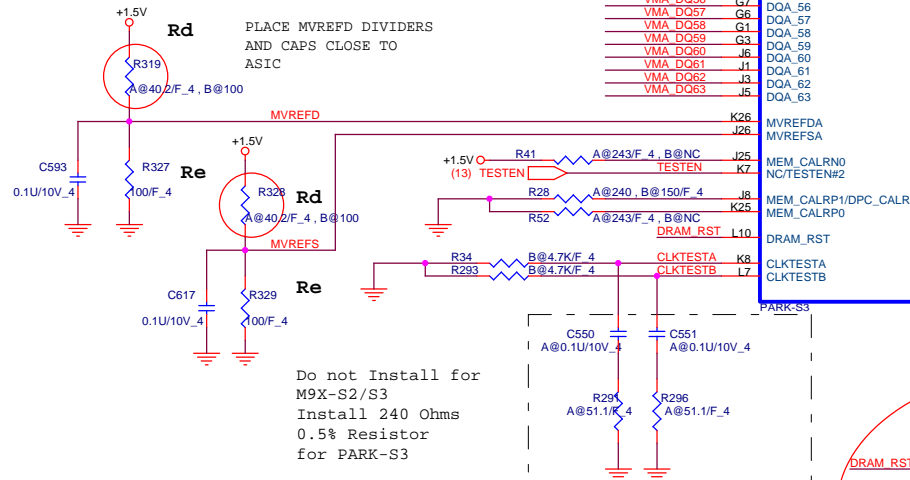
CKEA0 K20 VMA_CKE0
 CKEA1 J17 VMA_CKE1

WEA0B G25 VMA_WE0#
 WEA1B H10 VMA_WE1#

PX_EN AB16 VMA_MA13
 RSVD#2 G14 VMA_MA13
 RSVD#3 G20 VMA_MA13

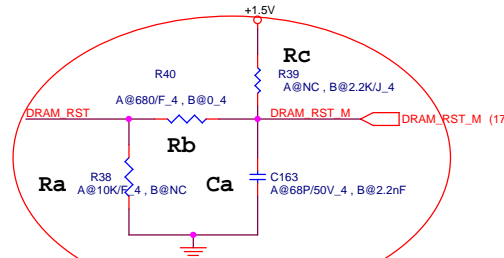
support 1Gbit VRAM (64M X 16)

A@ FOR PARK-S3
 B@ FOR M93



DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R

route 50ohms
single-ended/100ohms diff
and keep short



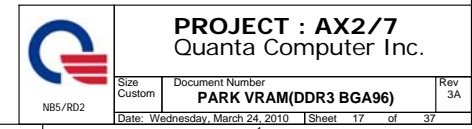
For PARK-S3 only
 For M9X-S2/S3 with
 DDR3: this pin is
 not in use.

Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	680R
Rc	2.2K	DNI
Ca	2.2nF	68pF

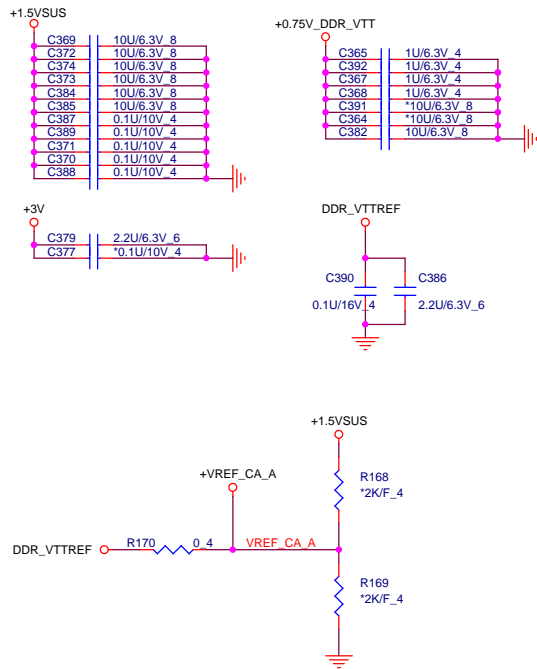


PROJECT : AX2/7
 Quanta Computer Inc.

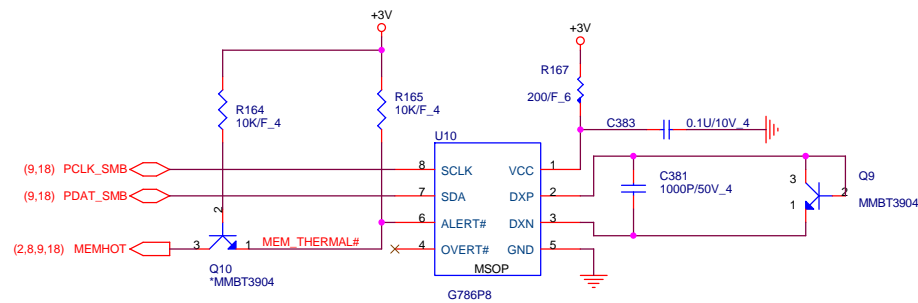
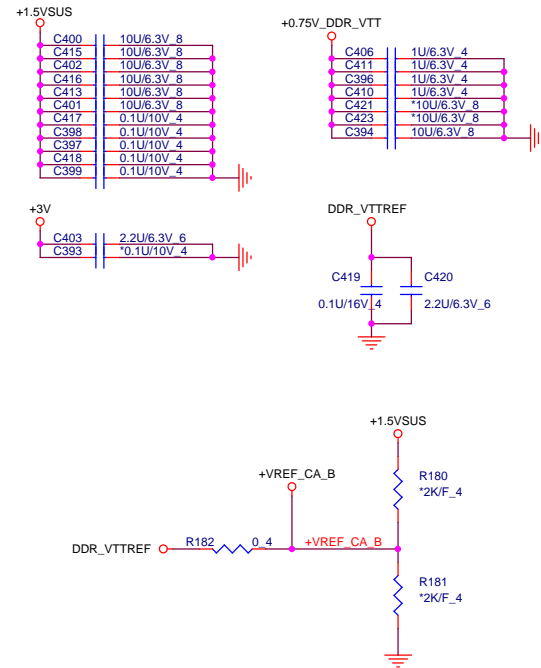
Size	Document Number	Rev
Custom	PARK/MEM_Interface	1A
Date: Wednesday, February 24, 2010	Sheet 16 of 37	



Place these Caps near So-Dimm0



Place these Caps near So-Dimm1



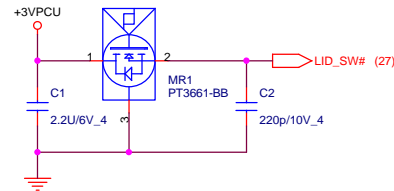
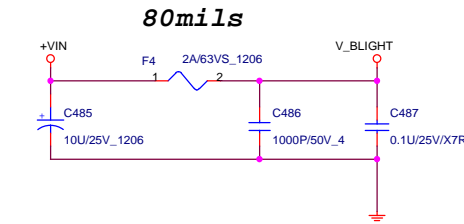
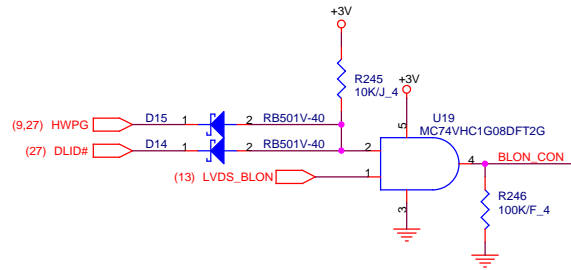
Quanta Computer Inc.

PROJECT :AMD Danube

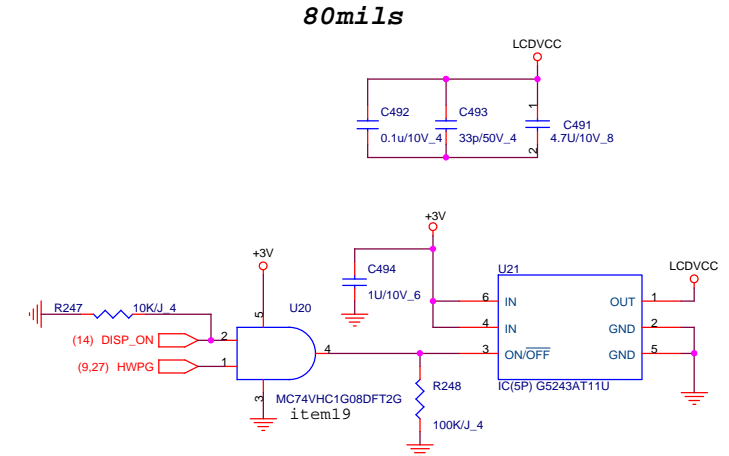
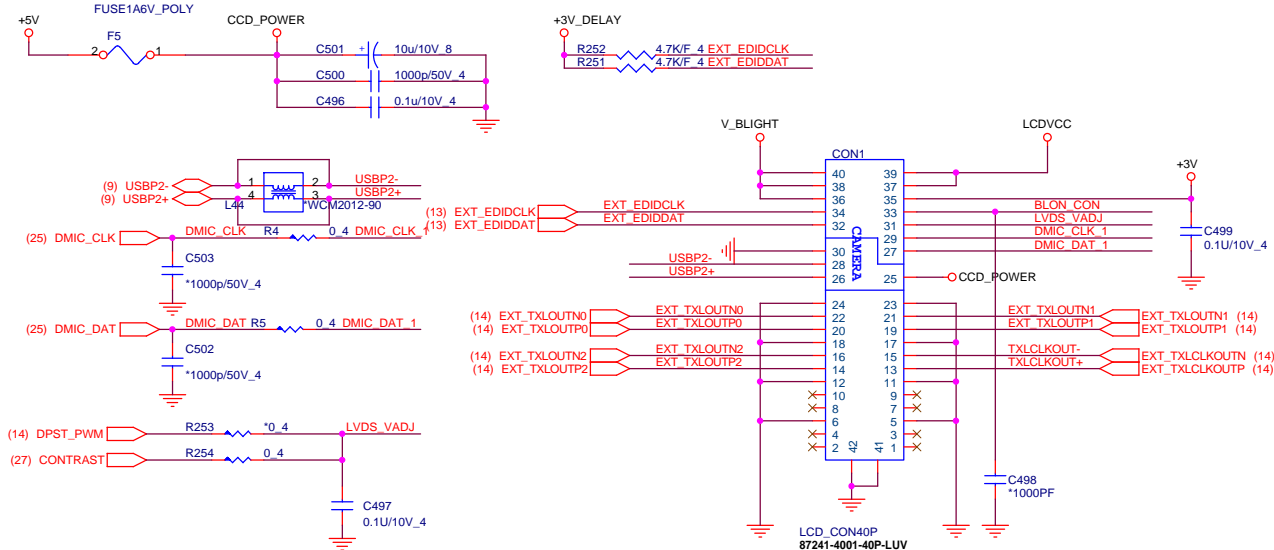
Size	Document Number	Rev
	DDR2 SODIMMS TERMINATIONS	1A

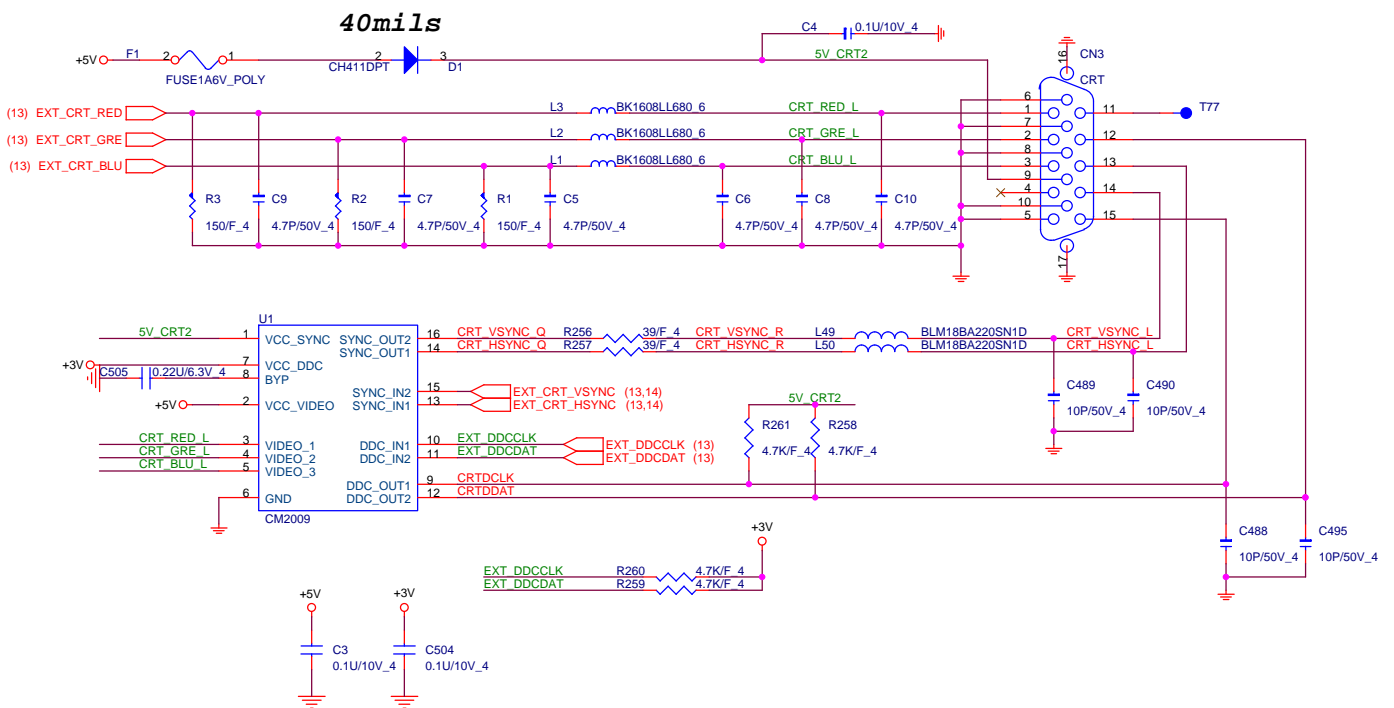
Date:	Wednesday, February 24, 2010	Sheet	19	of	37
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LID SW

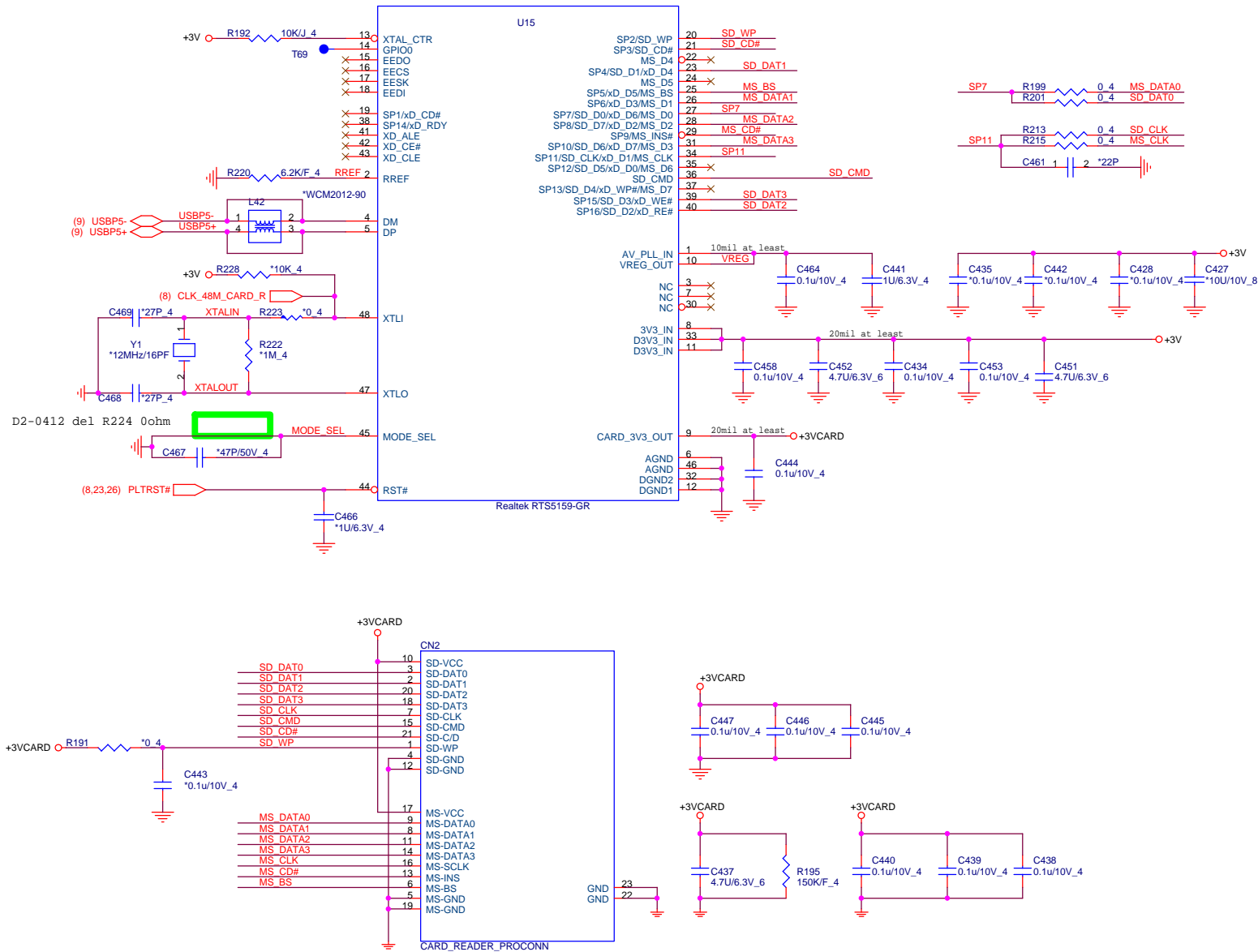


LVDS/CCD





Card Reader



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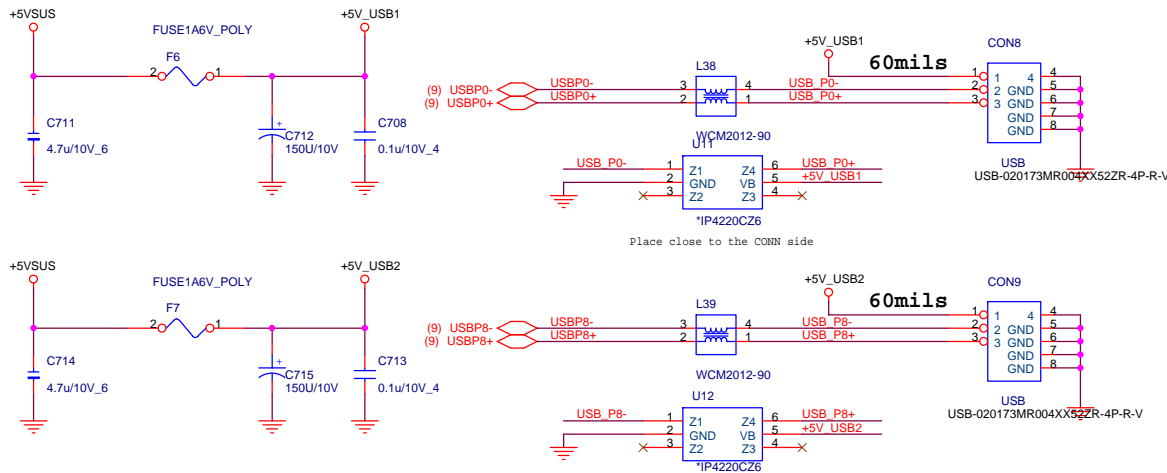
PROJECT : AMD Danube

Card Reader RT55159

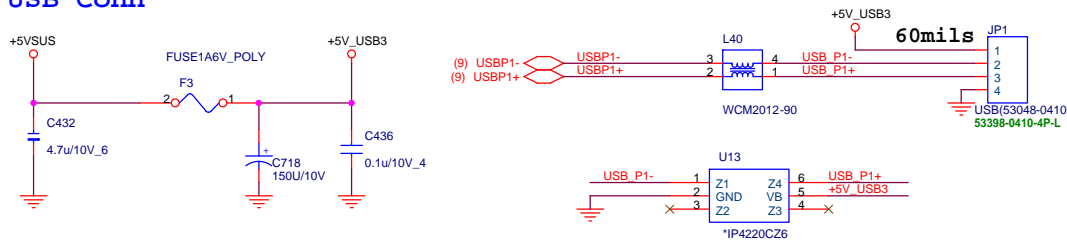
Size	Document Number	Rev
		1A

Date: Tuesday, April 20, 2010	Sheet 22 of 37
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USB PORTX2

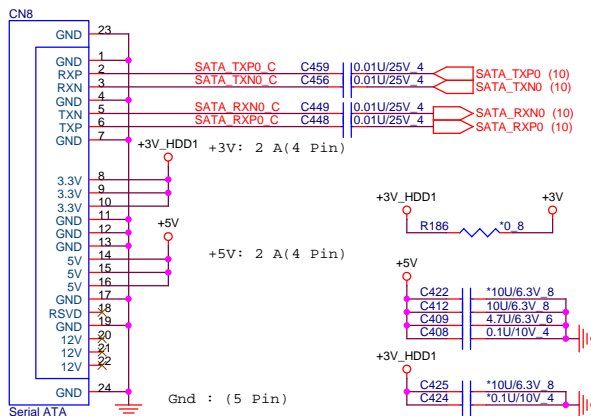


USB Conn



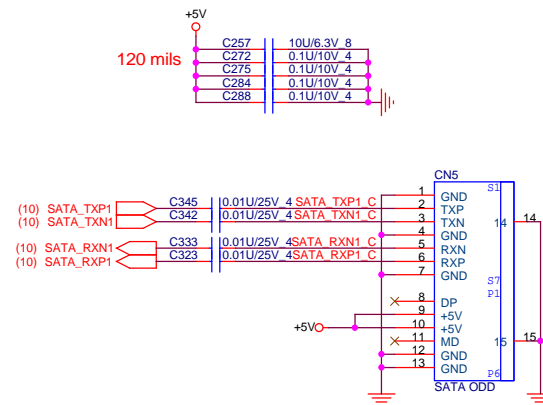
SATA HDD CONNECTOR

DC Current rating: 0.5 A



SATA CD-ROM

3V RUN Power.
Need Check
Net Name



Quanta Computer Inc.

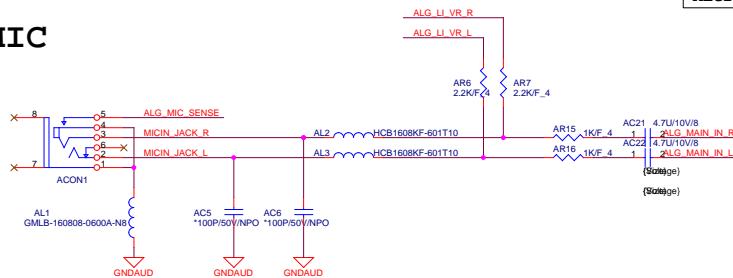
PROJECT : AMD Danube

USB Port/HDD/ODD

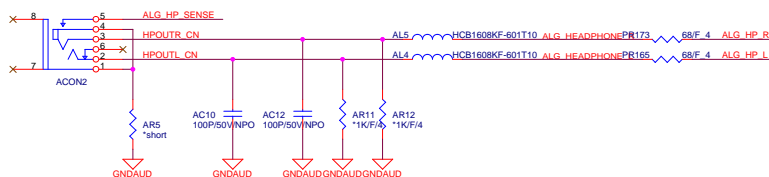
Size Document Number Rev 1A
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	Pa	Pb	Ac	Ra	Re	Ca	Cb	Cc	Dc	Dd	Da	Dd
ALC269Q-VA	×	×	×	×	×	×	×	×	×	×	×	×
ALC269Q-VB	×	×	×	×	×	×	×	×	×	×	×	×

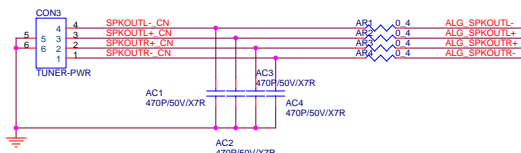
MIC



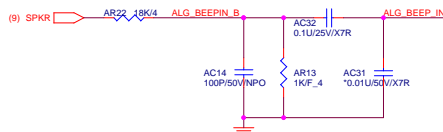
HP



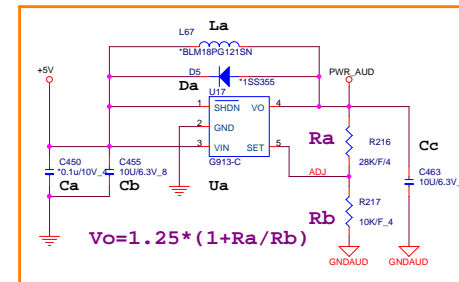
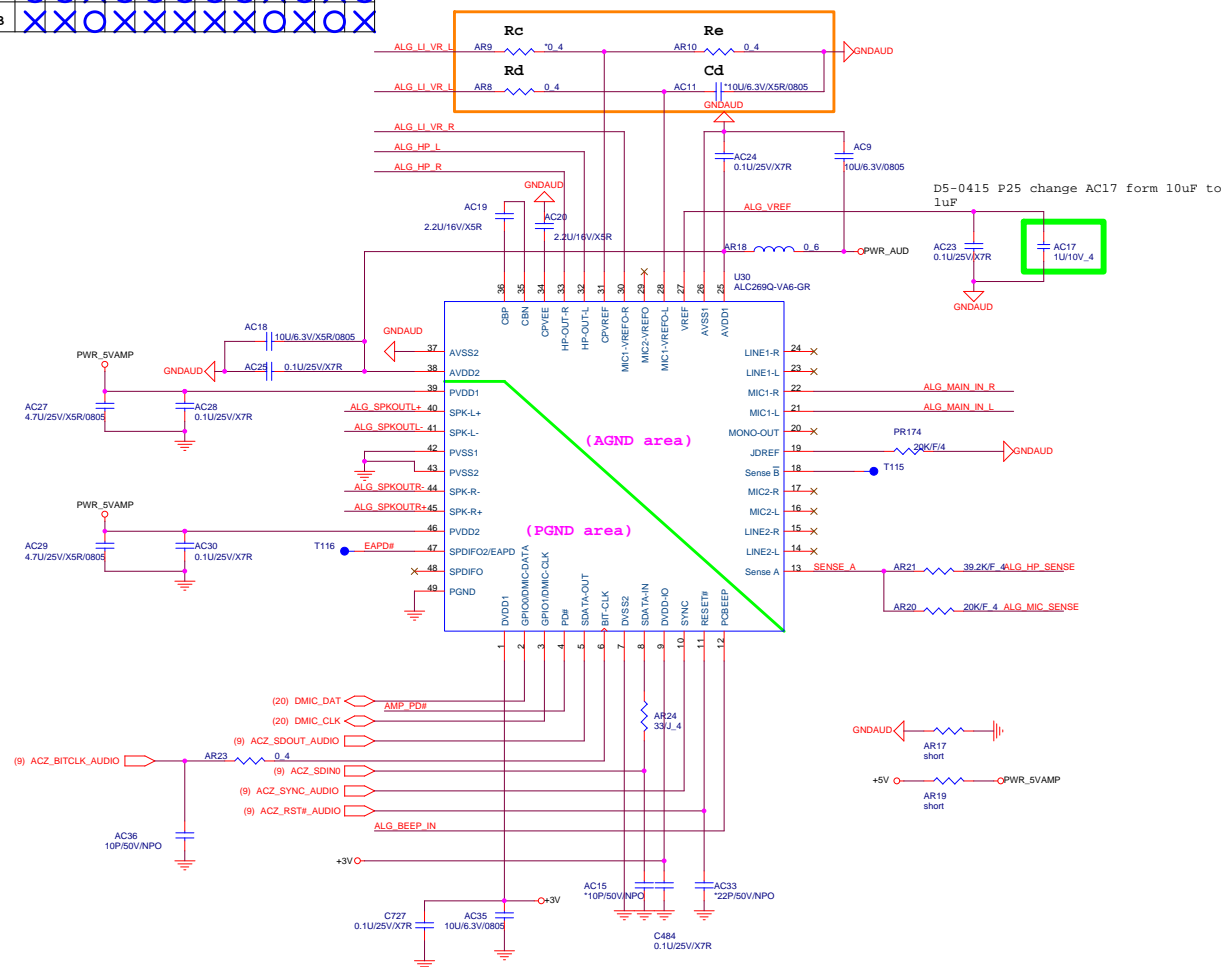
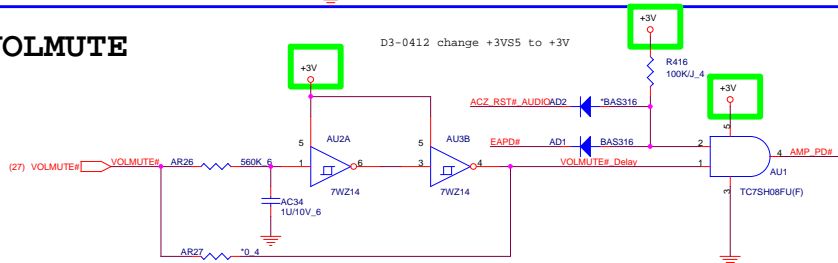
SPKR



BEEP



VOLMUTE



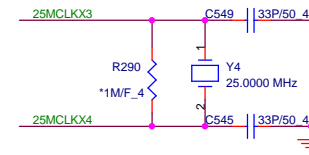
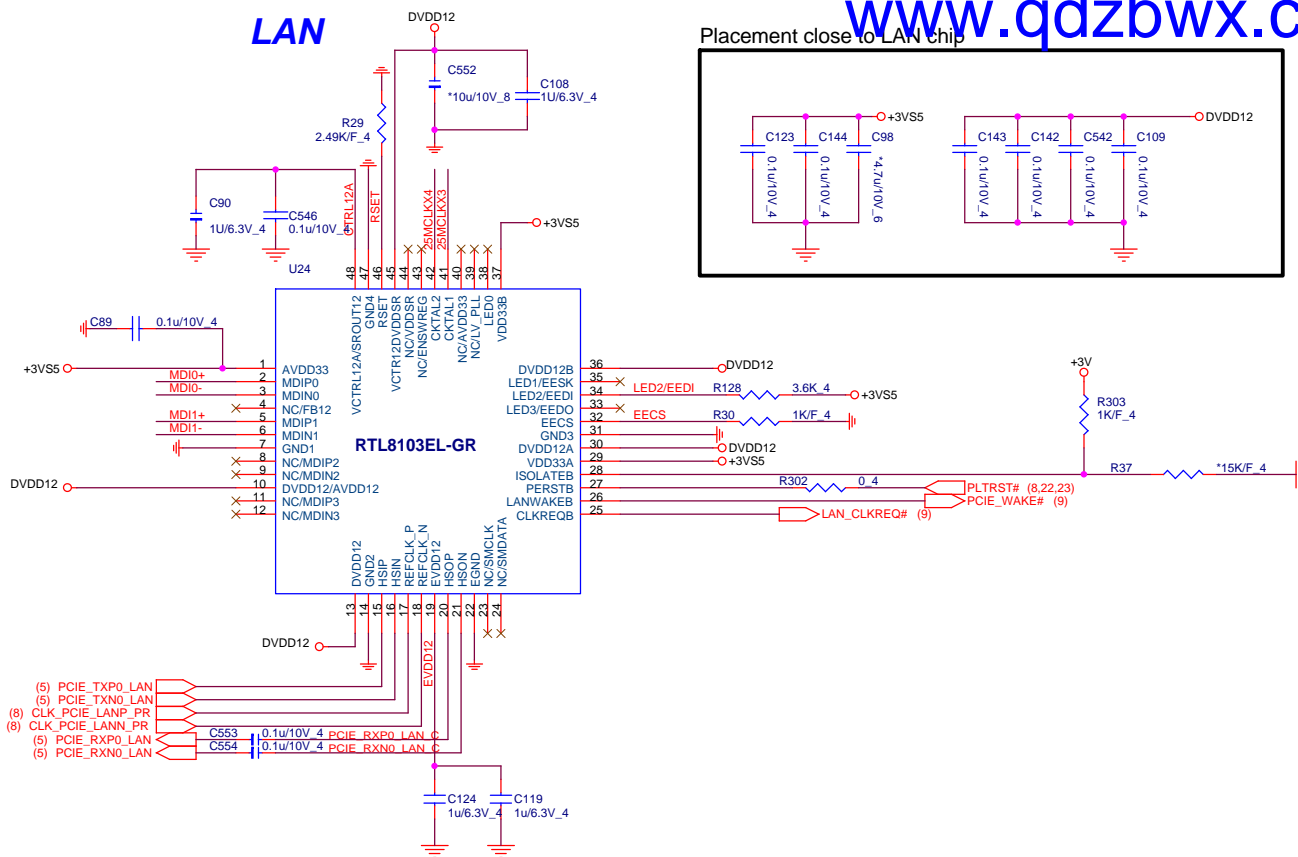
LAN

Placement close to LAN chip

www.qdzbxw.com

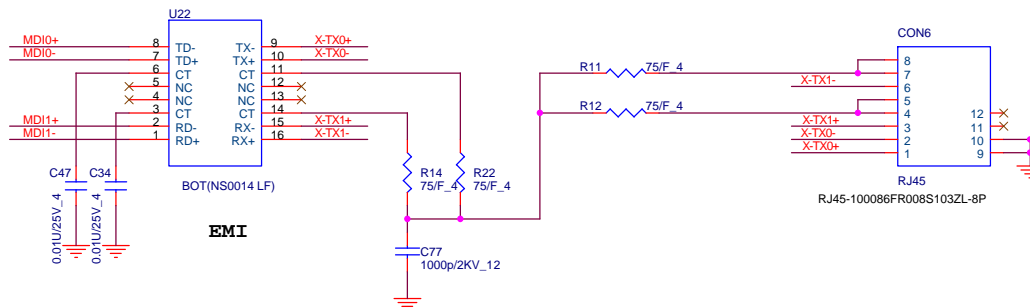
X'tal 25MHz

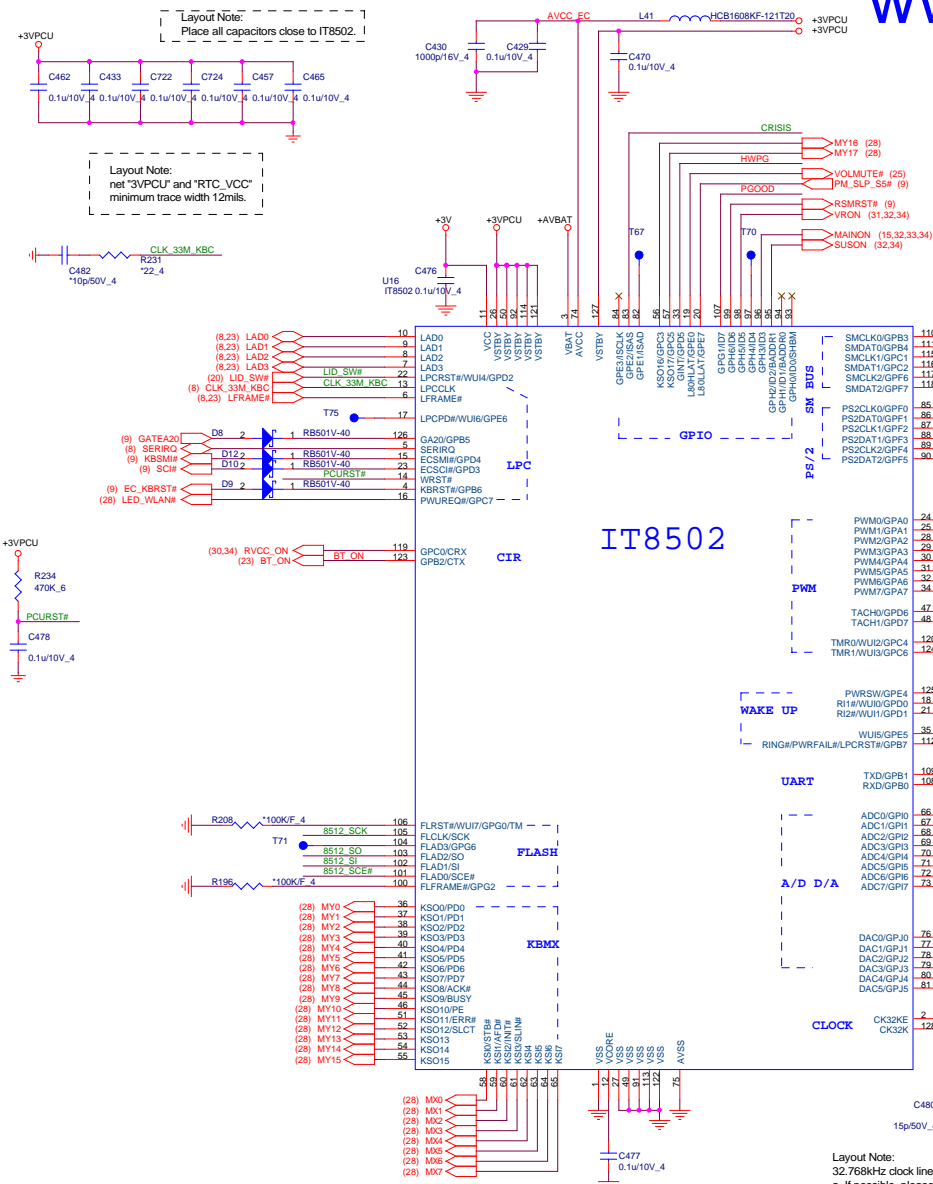
26



10/100 Transformer

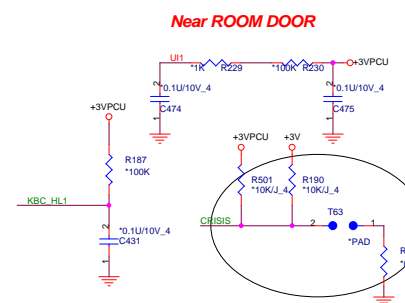
RJ45





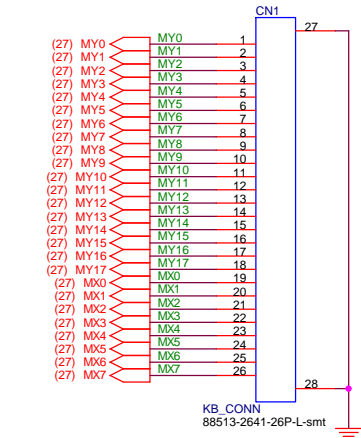
Layout Note:
32.768kHz clock lines:

- If possible, please avoid using any through-hole.
- Please make the trace length short, and the trace width wide enough.
- The spacing to the closest neighbor should be wide enough.



```
| 0415 , reserve circuit but
| SMT not mount
```

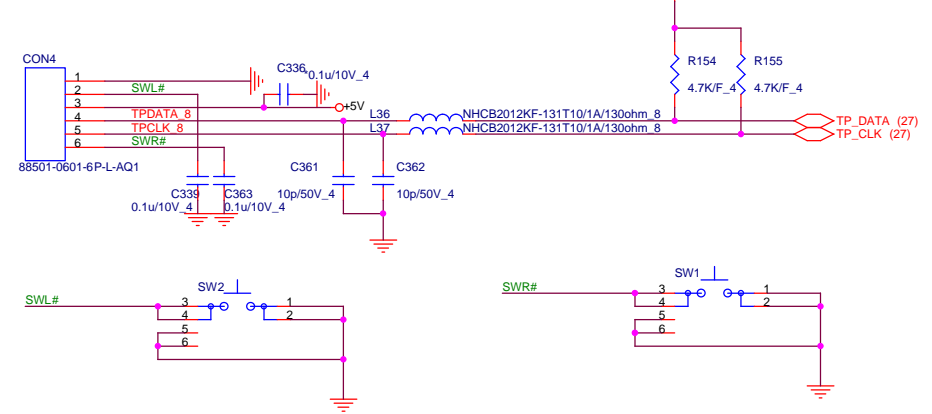
KEY BOARD



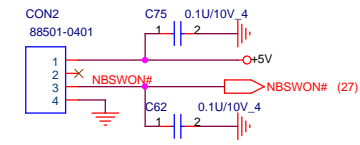
For EMI Reserve Caps for debug

MY3	C575	*10p/50V_4	C578	MX7
MY2	C576	*10p/50V_4	C579	MX6
MY1	C577	*10p/50V_4	C580	MX5
MY0	C558	*10p/50V_4	C581	MX4
MY15	C561	*10p/50V_4	C570	MY8
MY14	C562	*10p/50V_4	C569	MY9
MY13	C563	*10p/50V_4	C568	MY10
MY12	C564	*10p/50V_4	C567	MY11
MX0	C585	*10p/50V_4	C574	MY4
MX1	C584	*10p/50V_4	C573	MY5
MX2	C583	*10p/50V_4	C572	MY6
MX3	C582	*10p/50V_4	C571	MY7
MY16	C560	*10p/50V_4	C559	MY17

TOUCH PAD CONNECTOR

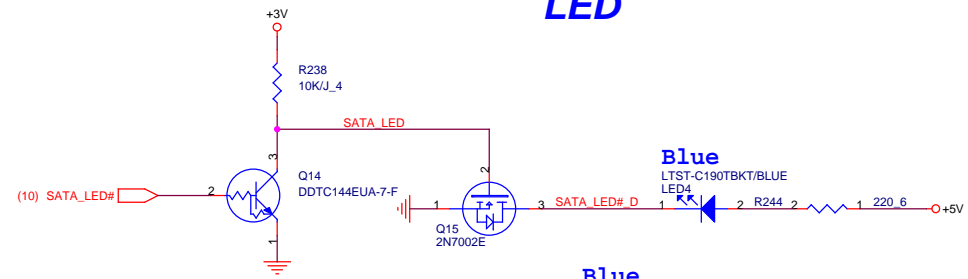


SW BOARD CON



LED

HDD/ODD



CAPS LED



NUM LED



WLAN

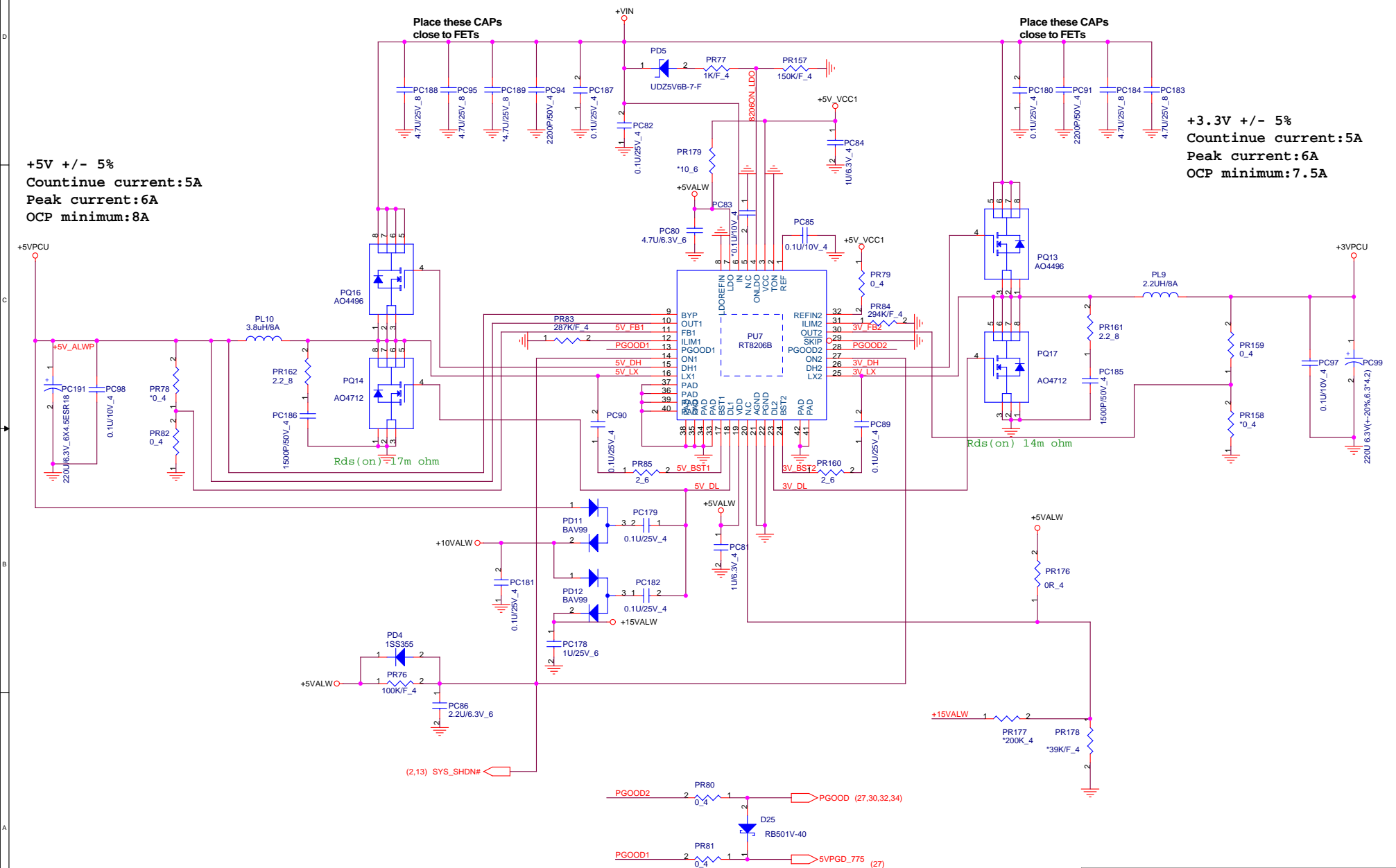


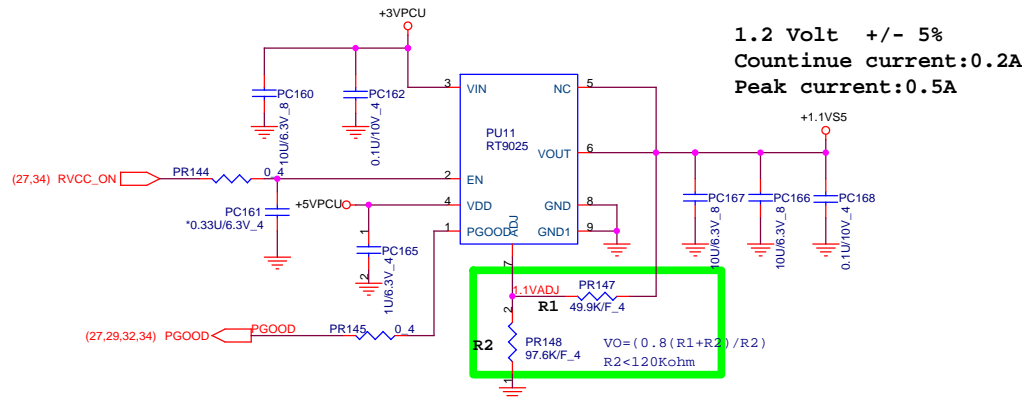
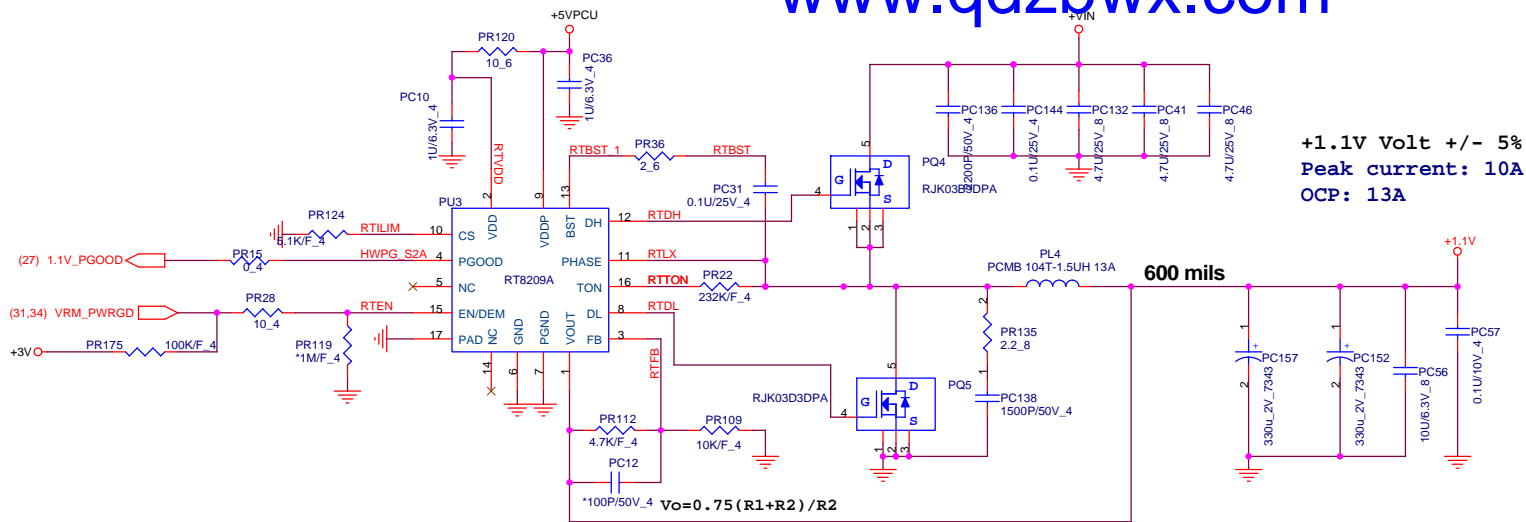
Battery



Power Status







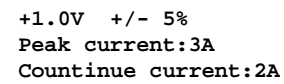
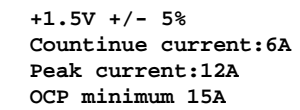
D4-0412 FOR AMD SB820M USB hold time issue on all
 Danubechange PR147 38.7K to 49.9K ohm
 change PR148 100K to 97.6K ohm



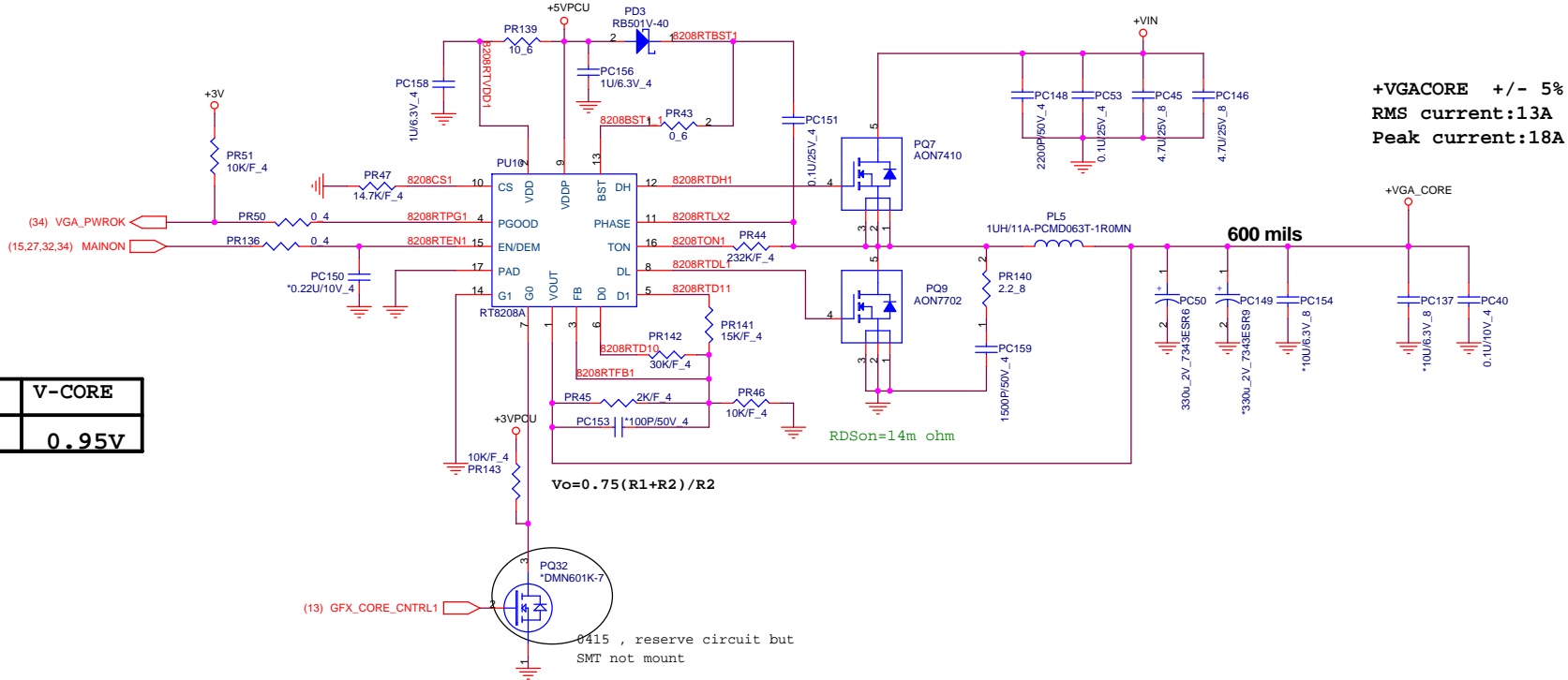
Quanta Computer Inc.

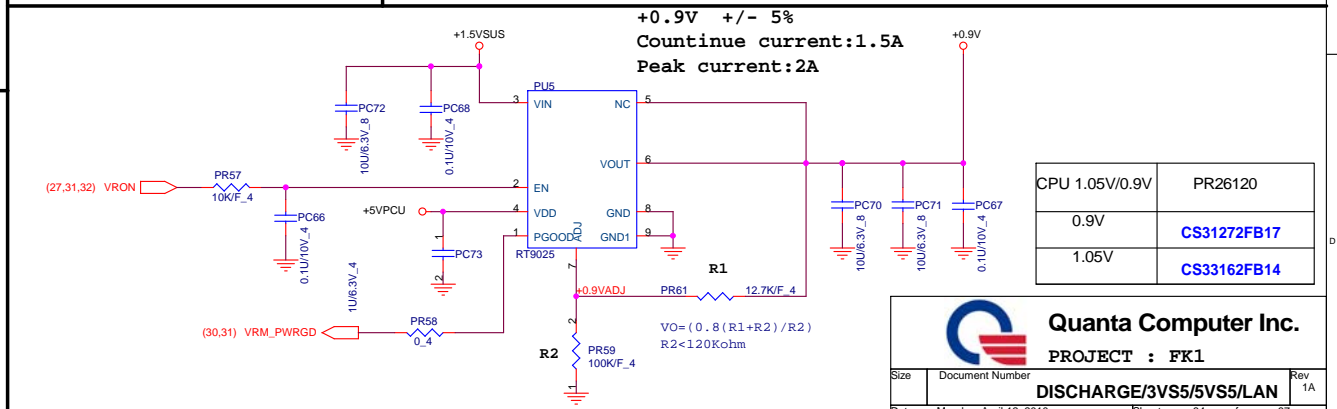
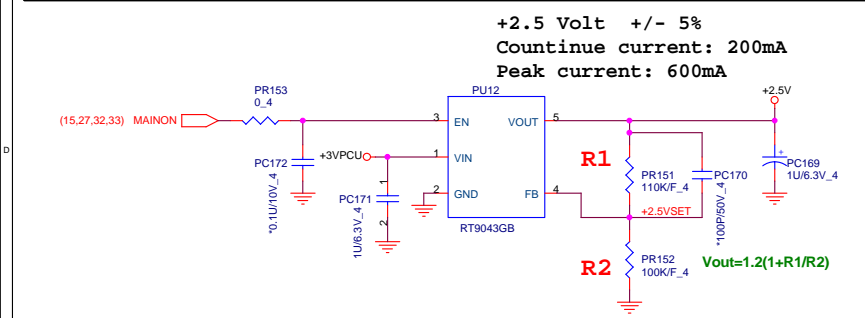
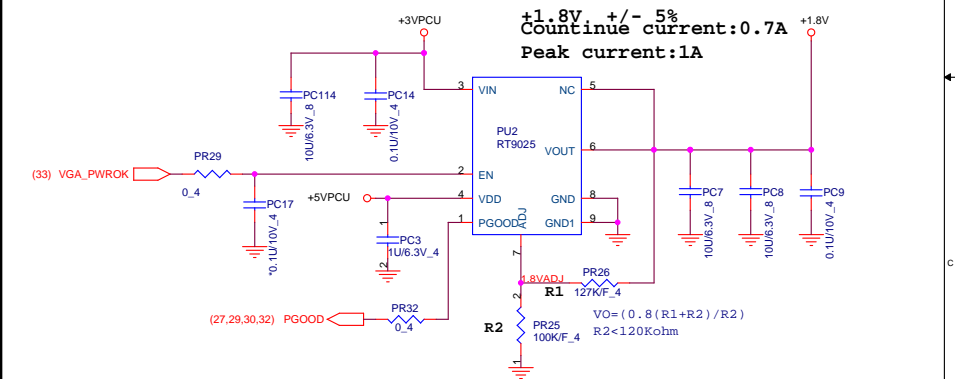
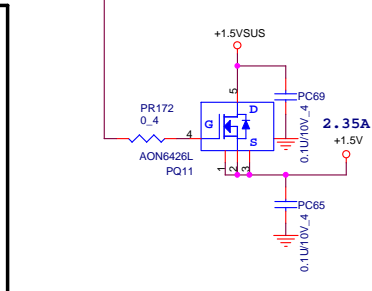
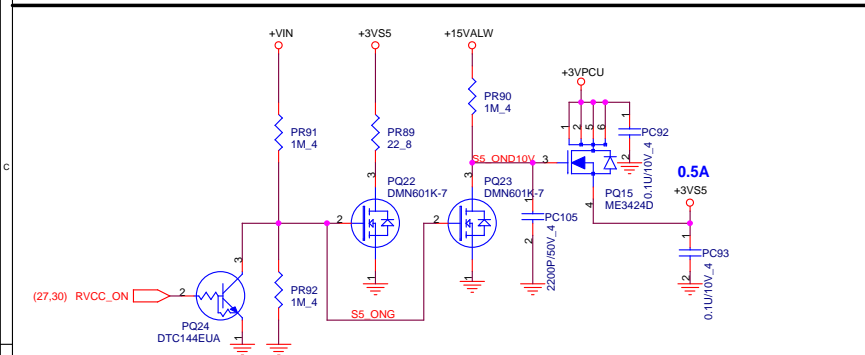
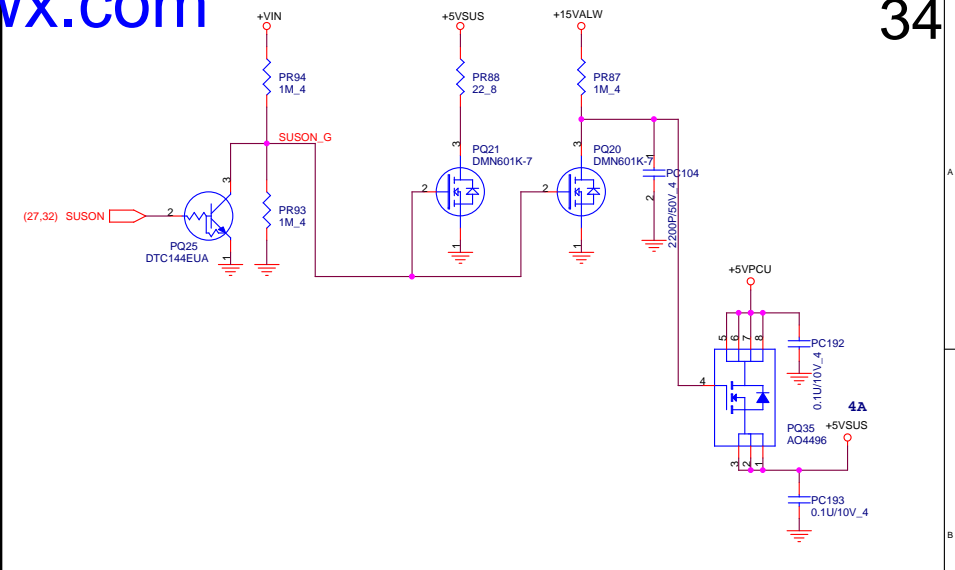
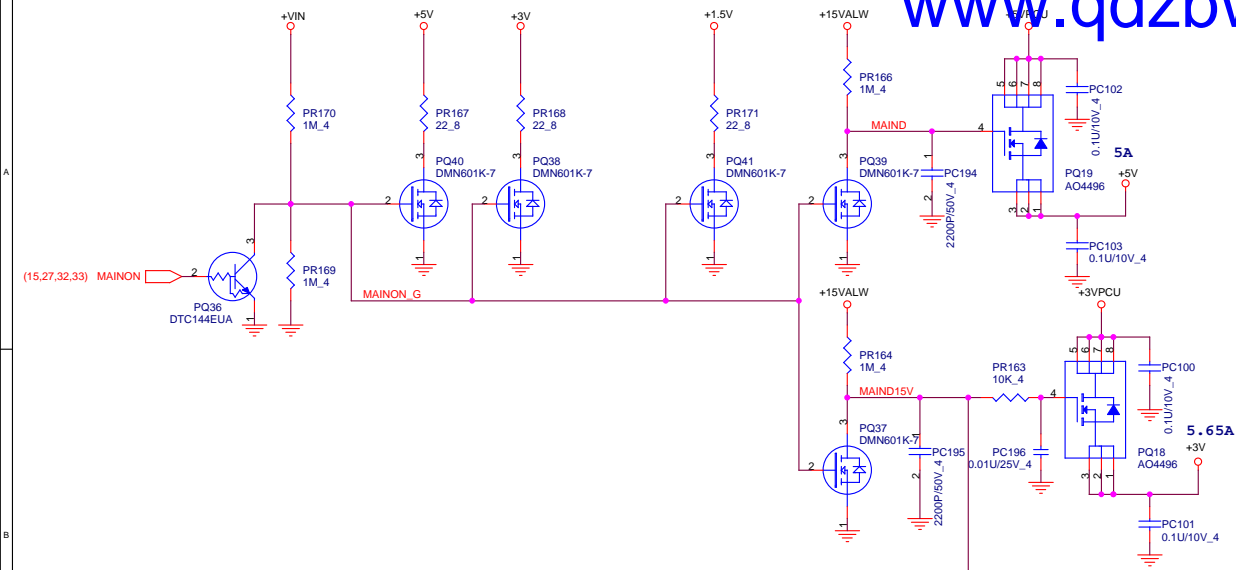
PROJECT : FK1

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G0	V-CORE
1	0.95V





CPU 1.05V/0.9V	PR26120
0.9V	CS31272FB17
1.05V	CS33162FB14



Quanta Computer Inc.

PROJECT : FK1

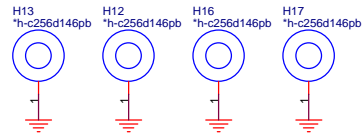
Size	Document Number	Rev
		1A

DISCHARGE/3VS5/5VS5/LAN

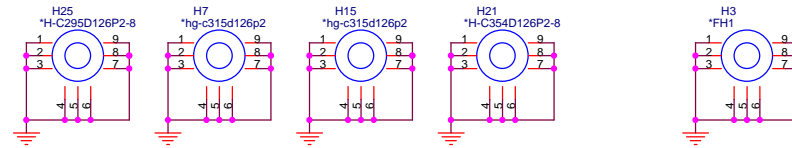
Date: Monday, April 12, 2010 Sheet 34 of 37

Hole

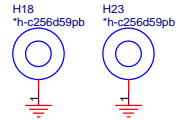
CPU Nut



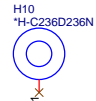
Hole for ESD



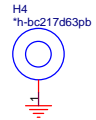
MINI CARD



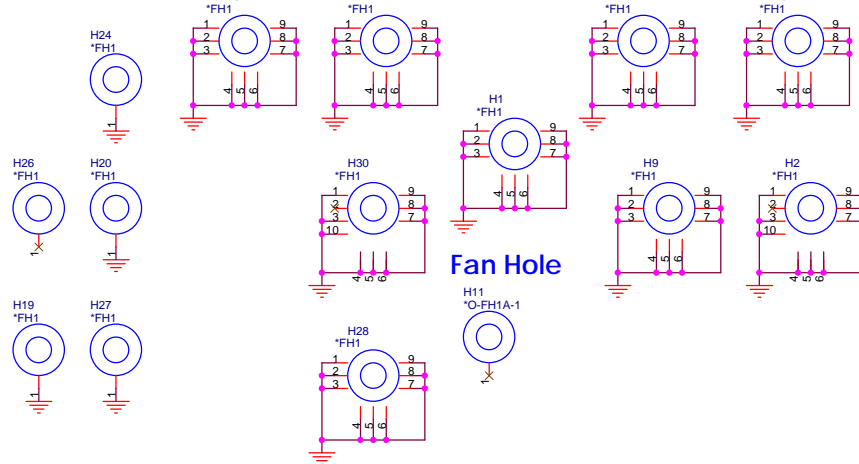
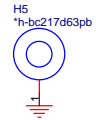
Antenna Hole



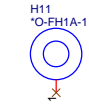
Thermal Module



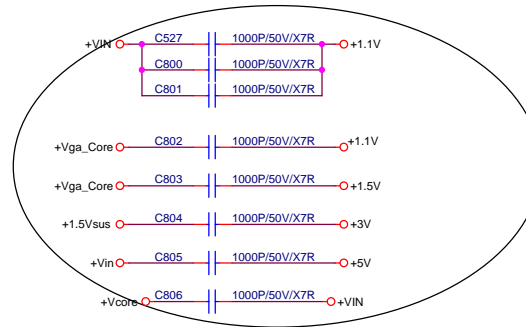
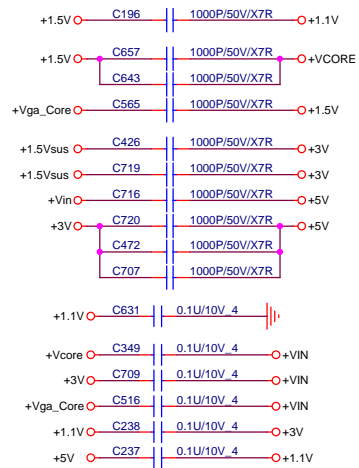
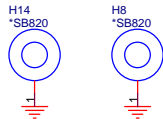
VGA Nut



Fan Hole



SB820



Change list from A to B stage

-P25 PR173,PR165 change to 68 ohm.
-P29 Add PR176,PR177,PR178
-P34 PR163 change from 0 to 10K ohm.(For power on timing)
-P34 Add PC196 0.01UF.(For power on timing)
-P34 PR29 change value from 49.9K to 0 ohm.(For Power on timing)
-P34 PC17 change value from 0.1U to NC.(Power on Timing)
-P36 Add C800 , C801 , C802 , C803 , C804, C805, C806
-P2 Add C760 , R500
-P29 delete PR86
-P30 PR124 ,PL4, PC31 change to 5.1K ,1.5UH ,0.1u for OCP 13A
-P31 PR4 change to NC
-P32 PC174 Mount
-P32 modify circuit for VDDIO_FB_H and VDDIO_FB_L
-P32 PR62 change to NC , delete PR123
-P33 PC153 Mount
-P34 Mount PR171 ,PQ41 ,PR88 ,PQ21 ,PR89 , PQ22 for discharge
-P34 delete PR10 , PR60
-P35 Mount PR14 , PR19 change form 10K to 100K
-P27 Add R501
-P27 Add D25

Change list from B to C stage

-P2 delete 0ohm R367 , R360 , R342
-P5 delete 0ohm R70
-P6 delete 0ohm R313 , R312 , R315 , R54
-P9 delete 0ohm R343 , R393 , R394
-P8 delete 0ohm RP1 , RP2 , RP3 , RP4 , RP5 , RP6 , RP7
-P20 delete 0ohm R250 , R249
-P22 delete 0ohm R219 , R205 , R225
-P26 delete 0ohm R203 , R301
-P25 delete 0ohm AR25
-Page 29,PC99 from Polymer capacitor change to E/C
-Page31,PQ8 and PQ31 low side Mosfet part number correct is RJK03D3DPA
-Page35 PL1 from 0805/5A change to 1206/6A

-P7 delete 0ohm L21 , L61 , L22 , R55 , R318 , R68 , R67
-P11 delete 0ohm R105 , R143 , L35 , R146 , L35 , R146 , R152

-P13 delete 0ohm R270 , R272 , R274
-P14 delete 0ohm R278 , R262

-P22 delete 0ohm R221 , R226 , R204 , R193 , R194 , R197 , R207
-P32 delete 0ohm PR72
-P20 C1 change form 0.1u to 2.2u
-P24 ADD L38,L39,L40 for EMI issue

Change list from C to MP stage

D1-P23 Delete R31 10Kohm , Delete U2 PIN1 trace
D2-P22 Delete R224 0ohm
D3-P25 change AU2 pin5 , AU3 pin5 , R416 pin1 , AU1 pin5 form +3VS5 to +3V

D4-P30 FOR AMD SB820M USB hold time issue on all Danube change PR147 38.7K to 49.9K ohm
change PR148 100K to 97.6K ohm

D5-P25 change AC17 form 10uF to 1uF

D6-P23 add C807 C808 10uF for VCC3_BT" dropped



Quanta Computer Inc.

PROJECT :AMD Danube

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